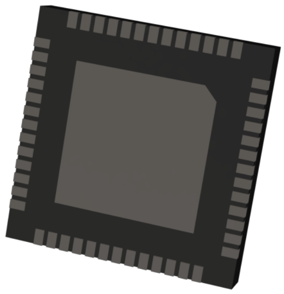
IQS9320 DATASHEET

Multi-Channel Inductive Sensing Device Aimed at Keyboard Applications

1 Device Overview

The IQS9320 ProxFusion® IC is a flexible multichannel inductive sensing device that supports a high number of channels per device, adjustable actuation points, analogue data streaming, and high report rates. The TriggerMax™ UI allows for dynamic actuation based on the distance a key is pressed or released. Other features include automatic tuning and long-term environmental tracking.

1.1 Main Features



- Up to 20 inductive sensors
- Up to 4 kHz sampling rate
- Per key adjustable actuation points
- Activation hysteresis
- TriggerMax™ dynamic actuation
- Sensor flexibility:
  - Automatic sensor tuning for optimal sensitivity
  - Internal voltage regulator
  - On-chip noise filtering
- RF immunity
- I^{2}C communication interface with IRQ/RDY, up to Fast-Mode Plus (1 MHz)
- Selectable I^{2}C addresses
- Analogue channel data streaming
- Multi-device matrix key scanning
- Multi-device synchronised sampling
- Automatic channel calibration
- Environmental tracking
- QFN52 (6×6×0.75 mm) – 0.4 mm pitch
- Wide input voltage supply range: 2.2 V to 3.5 V
- Wide operating temperature range: −40 °C to +85 °C

1.2 Applications

- Mechanical keyboards
- Waterproof buttons
- Remote controls
- Gaming controllers

1.3 System Overview

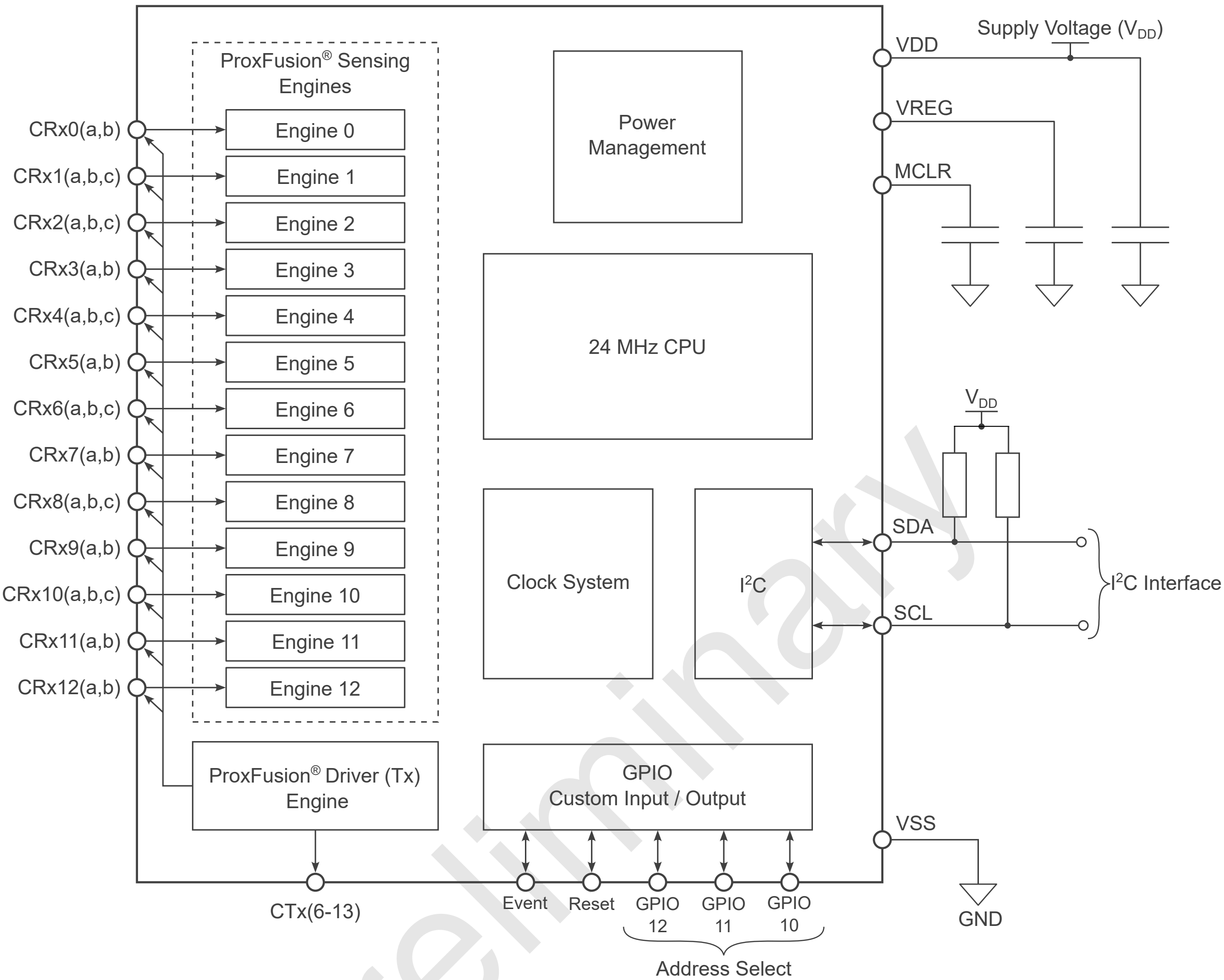


Figure 1.1: IQS9320 Block Diagram

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2 QFN52 Pinout

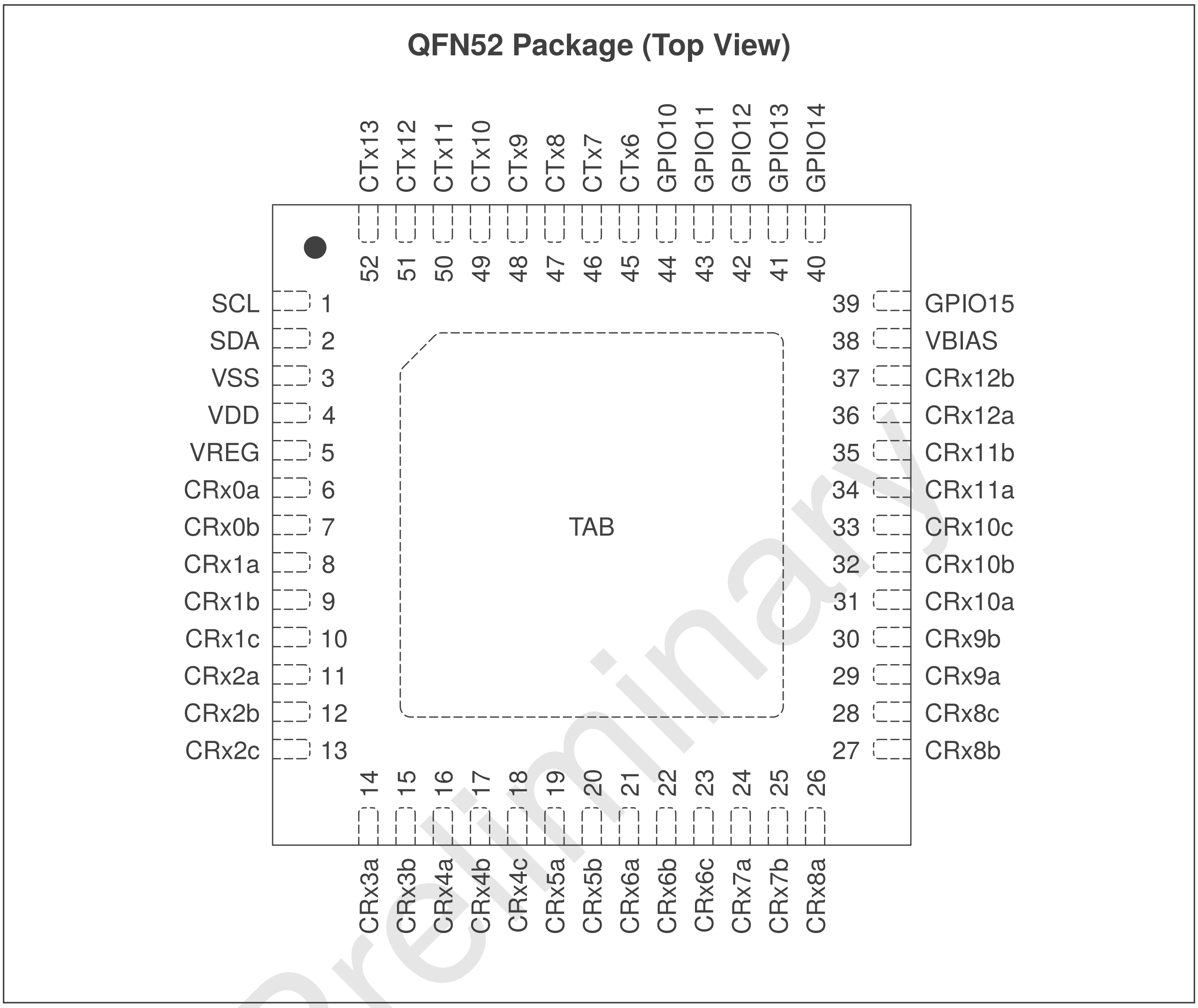

Figure 2.1: QFN52 Pinout

2.1 I²C Interface Configuration

Table 2.1: QFN52 Pin Descriptions

Pin	Name	Type(i)	Function	Description
1	SCL	I/O	I²C	I²C data
2	SDA	I/O	I²C	I²C clock
3	VSS	P	Power	Analog/digital ground
4	VDD	P	Power	Power supply input voltage
5	VREG	P	Power	Internally-regulated supply voltage
6	CRx0a	I/O	ProxFusion®	Inductive RX/TX
7	CRx0b	I/O	ProxFusion®	Inductive RX/TX
8	CRx1a	I/O	ProxFusion®	Inductive RX/TX

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Table 2.1: QFN52 Pin Descriptions (Continued)

Pin	Name	Type(i)	Function	Description
9	CRx1b	I/O	ProxFusion®	Inductive RX/TX
10	CRx1c	I/O	ProxFusion®	Inductive RX/TX
11	CRx2a	I/O	ProxFusion®	Inductive RX/TX
12	CRx2b	I/O	ProxFusion®	Inductive RX/TX
13	CRx2c	I/O	ProxFusion®	Inductive RX/TX
14	CRx3a	I/O	ProxFusion®	Inductive RX/TX
15	CRx3b	I/O	ProxFusion®	Inductive RX/TX
16	CRx4a	I/O	ProxFusion®	Inductive RX/TX
17	CRx4b	I/O	ProxFusion®	Inductive RX/TX
18	CRx4c	I/O	ProxFusion®	Inductive RX/TX
19	CRx5a	I/O	ProxFusion®	Inductive RX/TX
20	CRx5b	I/O	ProxFusion®	Inductive RX/TX
21	CRx6a	I/O	ProxFusion®	Inductive RX/TX
22	CRx6b	I/O	ProxFusion®	Inductive RX/TX
23	CRx6c	I/O	ProxFusion®	Inductive RX/TX
24	CRx7a	I/O	ProxFusion®	Inductive RX/TX
25	CRx7b	I/O	ProxFusion®	Inductive RX/TX
26	CRx8a	I/O	ProxFusion®	Inductive RX/TX
27	CRx8b	I/O	ProxFusion®	Inductive RX/TX
28	CRx8c	I/O	ProxFusion®	Inductive RX/TX
29	CRx9a	I/O	ProxFusion®	Inductive RX/TX
30	CRx9b	I/O	ProxFusion®	Inductive RX/TX
31	CRx10a	I/O	ProxFusion®	Inductive RX/TX
32	CRx10b	I/O	ProxFusion®	Inductive RX/TX
33	CRx10c	I/O	ProxFusion®	Inductive RX/TX
34	CRx11a	I/O	ProxFusion®	Inductive RX/TX
35	CRx11b	I/O	ProxFusion®	Inductive RX/TX
36	CRx12a	I/O	ProxFusion®	Inductive RX/TX
37	CRx12b	I/O	ProxFusion®	Inductive RX/TX
38	VBIAS	–	ProxFusion®	N/C
39	GPIO15	I	GPIO	MCLR
40	GPIO14	O	GPIO	Event Pin
41	GPIO13	O	GPIO	Reset Pin
42	GPIO12	I	GPIO	I²C Address Select 0
43	GPIO11	I	GPIO	I²C Address Select 1
44	GPIO10	I	GPIO	I²C Address Select 2
45	CTx6	O	ProxFusion®	Inductive TX

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Table 2.1: QFN52 Pin Descriptions (Continued)

Pin	Name	Type(i)	Function	Description
46	CTx7	O	ProxFusion®	Inductive TX
47	CTx8	O	ProxFusion®	Inductive TX
48	CTx9	O	ProxFusion®	Inductive TX
49	CTx10	O	ProxFusion®	Inductive TX
50	CTx11	O	ProxFusion®	Inductive TX
51	CTx12	O	ProxFusion®	Inductive TX/ External POSC Clock Output
52	CTx13	I/O	ProxFusion®	Inductive TX/ External POSC Clock Input

i Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

2.2 GPIO Interface Configuration

Table 2.2: QFN52 Pin Descriptions

Pin	Name	Type(i)	Function	Description
1	SCL	I/O	I^2C	I^2C data
2	SDA	I/O	I^2C	I^2C clock
3	VSS	P	Power	Analog/digital ground
4	VDD	P	Power	Power supply input voltage
5	VREG	P	Power	Internally-regulated supply voltage
6	CRx0a	I/O	ProxFusion®	Inductive RX/TX
7	CRx0b	I/O	ProxFusion®	Inductive RX/TX
8	CRx1a	I/O	ProxFusion®	Inductive RX/TX
9	CRx1b	I/O	ProxFusion®	Inductive RX/TX
10	CRx1c	I/O	ProxFusion®	Inductive RX/TX
11	CRx2a	I/O	ProxFusion®	Inductive RX/TX
12	CRx2b	I/O	ProxFusion®	Inductive RX/TX
13	CRx2c	I/O	ProxFusion®	Inductive RX/TX
14	CRx3a	I/O	ProxFusion®	Inductive RX/TX
15	CRx3b	I/O	ProxFusion®	Inductive RX/TX
16	CRx4a	I/O	ProxFusion®	Inductive RX/TX
17	CRx4b	I/O	ProxFusion®	Inductive RX/TX
18	CRx4c	I/O	ProxFusion®	Inductive RX/TX
19	CRx5a	I/O	ProxFusion®	Inductive RX/TX
20	CRx5b	I/O	ProxFusion®	Inductive RX/TX
21	CRx6a	I/O	ProxFusion®	Inductive RX/TX
22	CRx6b	I/O	ProxFusion®	Inductive RX/TX
23	CRx6c	I/O	ProxFusion®	Inductive RX/TX
24	CRx7a	I/O	ProxFusion®	Inductive RX/TX

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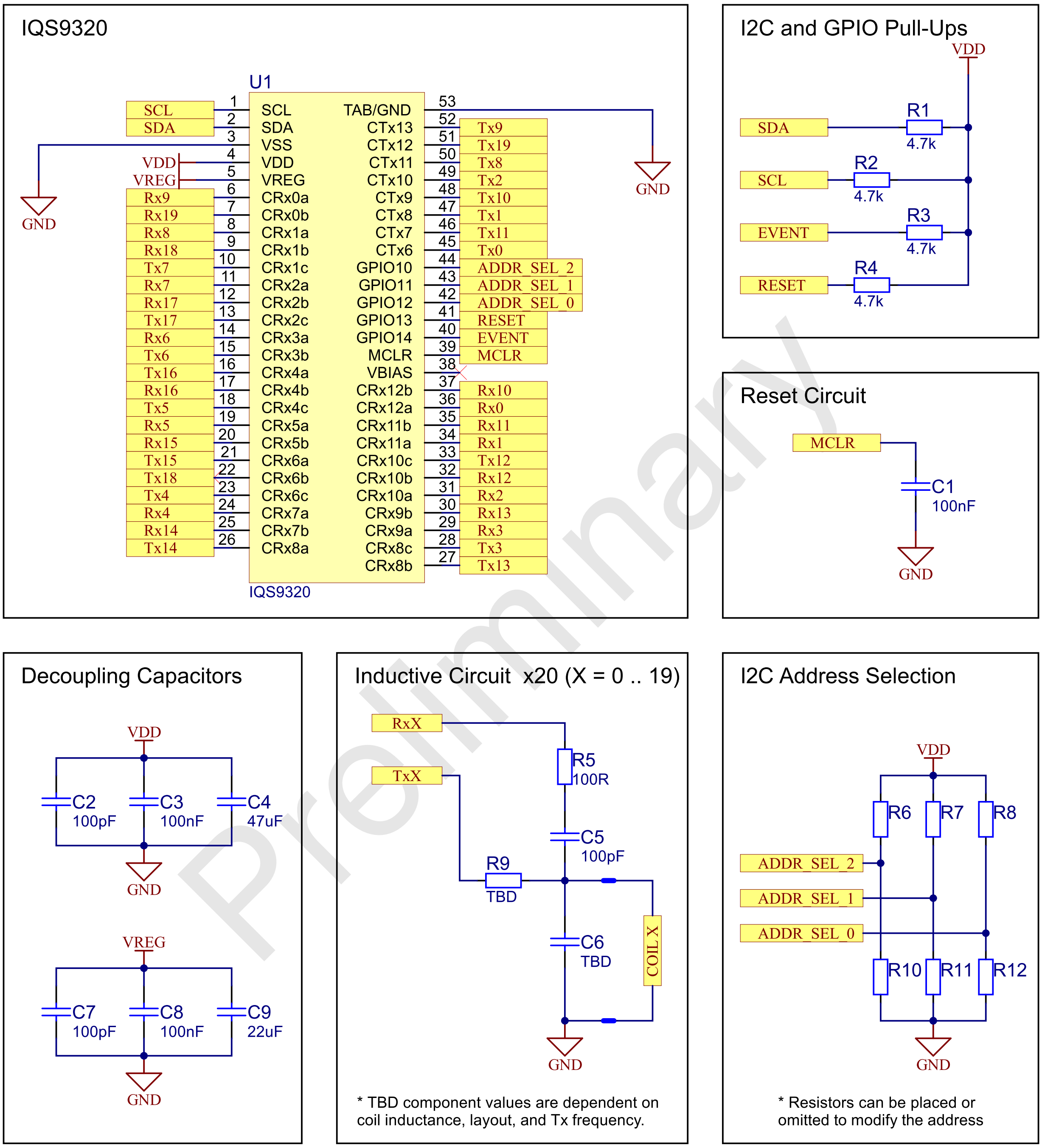
Table 2.2: QFN52 Pin Descriptions (Continued)

Pin	Name	Type(i)	Function	Description
25	CRx7b	I/O	ProxFusion®	Inductive RX/TX
26	CRx8a	I/O	ProxFusion®	Inductive RX/TX
27	CRx8b	I/O	ProxFusion®	Inductive RX/TX
28	CRx8c	I/O	ProxFusion®	Inductive RX/TX
29	CRx9a	I/O	ProxFusion®	Inductive RX/TX
30	CRx9b	I/O	ProxFusion®	Inductive RX/TX
31	CRx10a	I/O	ProxFusion®	Inductive RX/TX
32	CRx10b	I/O	ProxFusion®	Inductive RX/TX
33	CRx10c	I/O	ProxFusion®	Inductive RX/TX
34	CRx11a	I/O	ProxFusion®	Inductive RX/TX
35	CRx11b	I/O	ProxFusion®	Inductive RX/TX
36	CRx12a	I/O	ProxFusion®	Inductive RX/TX
37	CRx12b	I/O	ProxFusion®	Inductive RX/TX
38	VBIAS	–	ProxFusion®	N/C
39	GPIO15	I	GPIO	MCLR
40	GPIO14	I/O	GPIO	C0
41	GPIO13	I/O	GPIO	R0
42	GPIO12	O	GPIO	R1
43	GPIO11	O	GPIO	R2
44	GPIO10	I/O	GPIO	R3
45	CTx6	O	ProxFusion®	Inductive TX
46	CTx7	O	ProxFusion®	Inductive TX
47	CTx8	O	ProxFusion®	Inductive TX
48	CTx9	O	ProxFusion®	Inductive TX
49	CTx10	O	ProxFusion®	Inductive TX
50	CTx11	O	ProxFusion®	Inductive TX
51	CTx12	O	ProxFusion®	Inductive TX/ External POSC Clock Output
52	CTx13	I/O	ProxFusion®	Inductive TX/ External POSC Clock Input

i Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

3 Reference Schematic

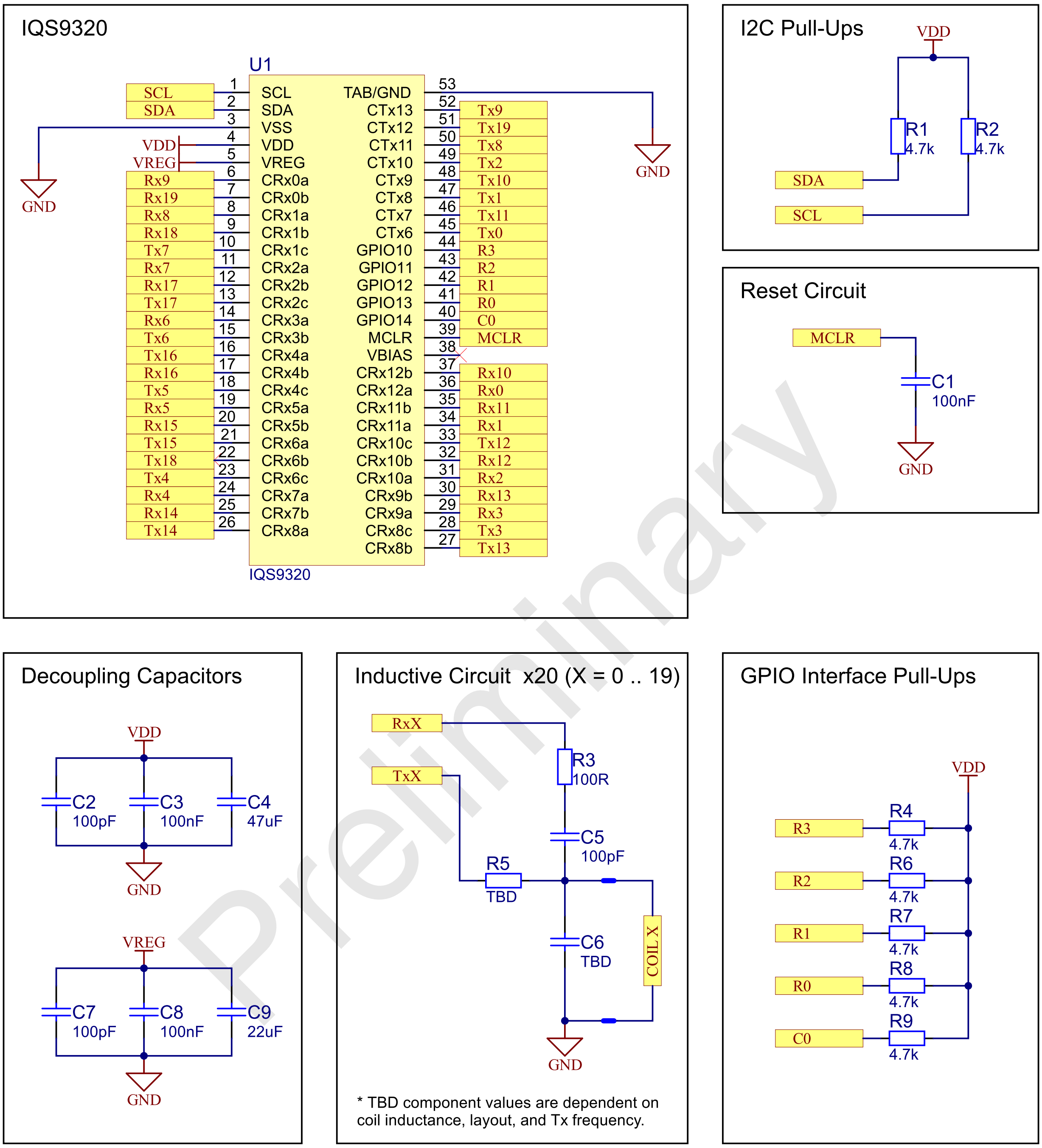
3.1 I²C Interface Configuration



* Schematic subject to change without notice

Figure 3.1: IQS9320 Reference Schematic with Selectable I²C Address

3.2 GPIO Interface Configuration



* Schematic subject to change without notice

Figure 3.2: IQS9320 Reference Schematic with Keyscanning

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4.1: Absolute Maximum Ratings

Symbol	Rating	Min	Max	Unit
V_{DD}	Voltage applied at VDD pin (referenced to VSS)	−0.3	3.5	V
V_{IN}	Voltage applied to any ProxFusion® pin (referenced to VSS)	−0.3	V_{REG}	V
	Voltage applied to any other pin (referenced to VSS)	−0.3	V_{DD} + 0.3 (3.5 V max)	V
T_{stg}	Storage temparature	−40	85	°C

4.2 General Operating Conditions

Table 4.2: General Operating Conditions

Symbol	Parameter	Typ	Unit
F_{OSC}	Master clock frequency	24	MHz
F_{POSC}	ProxFusion® engine clock frequency	16	MHz
V_{REG}	Internally-regulated supply output	1.80	V

4.3 ESD Rating

Table 4.3: ESD Rating

			Value	Unit
$V_{(ESD)}$	Electrostatic discharge voltage	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[i]	±2000	V

[i] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

4.4 Reset Levels

Table 4.4: Reset Levels

Parameter		Min	Typ	Max	Unit
VDD	Power-up (Reset trigger) – slope > 100 V/s	1.65			V
	Power-down (Reset trigger) – slope < −100 V/s			0.9	

4.5 MCLR Pin Levels and Characteristics

Table 4.5: MCLR Pin Characteristics

Parameter		Min	Typ	Max	Unit
V_{IL}	MCLR input low level voltage	V_{SS} – 0.3		0.25 × V_{DD}	V
V_{IH}	MCLR input high level voltage	0.75 × V_{DD}		V_{DD} + 0.3	V
R_{PU}	MCLR pull-up equivalent resistor		210		kΩ
t_{Trig}	MCLR input pulse width – ensure trigger	250			ns

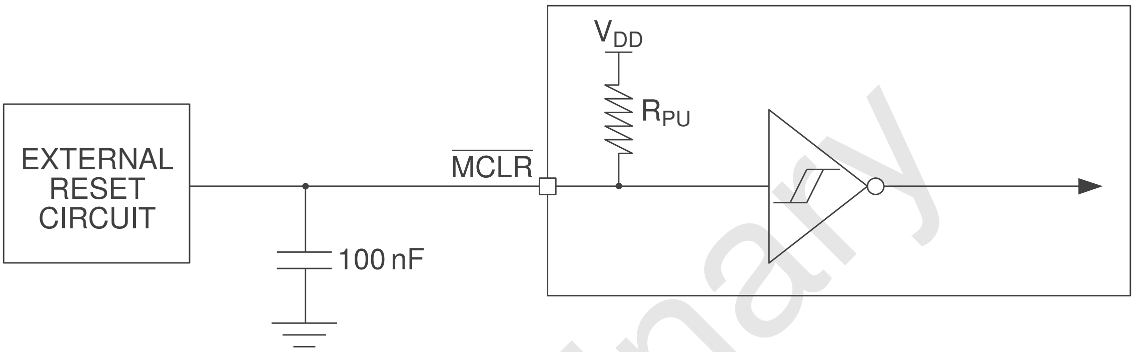


Figure 4.1: MCLR Pin Diagram

4.6 Recommended Operating Conditions

Table 4.6: Recommended Operating Conditions

Symbol	Parameter	Min	Recommended	Max	Unit
V_{DD}	Standard operating voltage, applied at VDD pin	2.2		3.5	V
T_A	Operating free-air temperature	−20		85	°C
C_{VDD}	Recommended capacitor at VDD	C_{VREG}	2×C_{VREG}		µF
C_{VREG}	Recommended external buffer capacitor at VREG (ESR ≤ 200 mΩ)	10[i]	22	88	µF

[i] Absolute minimum allowed capacitance value is 4.7 µF, after derating for voltage, temperature, and worst-case tolerance.

4.7 ProxFusion® Electrical Characteristics

Table 4.7: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU,STA}$	Set-up time for a repeated START condition	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data set-up time	50		ns
$t_{SU,STO}$	Set-up time for STOP condition	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

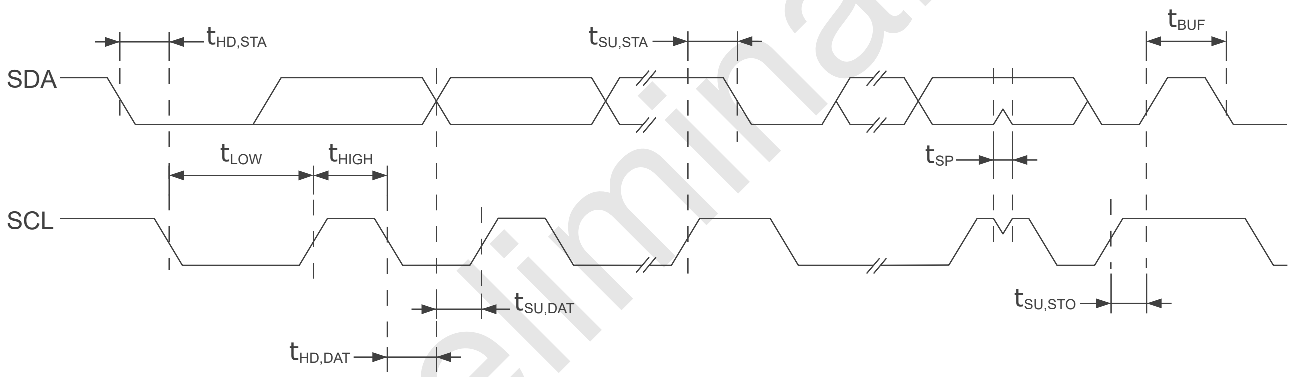


Figure 4.2: I²C Timing Diagram

4.8 Current consumption

The current draw of the IQS9320 is defined by the selected communication method, the number of channels being sampled, and the sample rate of the active power mode. All current measurements were taken with an ATI target of 1023, a Tx frequency of 16MHz, and a conversion frequency of 8MHz.

Table 4.8: Current Consumption

Mode	Number of Channels	Sample Interval [ms]	Average Current Consumption [µA]
I^2C Interface	20	0.73	6660
I^2C Interface	20	5	1790
I^2C Interface	20	20	600
I^2C Interface	20	50	250
I^2C Interface	20	100	125
I^2C Interface	10	0.43	6420
I^2C Interface	10	5	1520
I^2C Interface	10	20	510
I^2C Interface	10	50	210
I^2C Interface	10	100	105
I^2C Interface	4	0.20	5940
I^2C Interface	4	5	1210
I^2C Interface	4	20	450
I^2C Interface	4	50	180
I^2C Interface	4	100	90
GPIO Interface	20	0.73	6450
GPIO Interface	20	5	2180
GPIO Interface	20	20	1550
GPIO Interface	20	50	1400
GPIO Interface	20	100	1350
GPIO Interface	10	0.43	6270
GPIO Interface	10	5	1940
GPIO Interface	10	20	1470
GPIO Interface	10	50	1370
GPIO Interface	10	100	1330
GPIO Interface	4	0.2	5840
GPIO Interface	4	5	1640
GPIO Interface	4	20	1250
GPIO Interface	4	50	1170
GPIO Interface	4	100	1140
Standby	-	-	3

5 Application and Implementation

5.1 Sampling Rate

The maximum sampling rate of the IQS9320 is defined by the number of channels, the value of the raw counts sampled, the selected communication method, and the number of activated channels being sampled. Activated channels are channels for which the *Normalised Delta* has exceeded the *Activation Threshold* to indicate a key press from a user. The device requires some additional processing to manage activated channels. The additional sample time required for a given communications method is the time required by the IQS9320 to process communications if communications occur for each sample.

Table 5.1: Sampling Rate for Streaming

Number of Channels	Activated Channels	Raw Counts	Sample Time [µs]	Sample Time (I^2C) [µs]	Sample Rate (I^2C) [kHz]	Sample Time (Key Scan) [µs]	Sample Rate (Key Scan) [kHz]
20	20	1023	820	860	1.16	920	1.09
20	0	1023	760	800	1.25	860	1.16
20	20	383	800	840	1.19	900	1.11
20	0	383	760	800	1.25	860	1.16
16	16	1023	700	740	1.35	785	1.27
16	0	1023	620	660	1.52	705	1.42
16	16	383	660	700	1.43	745	1.34
16	0	383	620	660	1.52	705	1.42
12	12	1023	560	600	1.66	630	1.59
12	0	1023	500	540	1.85	570	1.75
12	12	383	490	530	1.89	560	1.79
12	0	383	470	510	1.96	540	1.85
8	8	1023	430	470	2.13	485	2.06
8	0	1023	390	430	2.32	445	2.25
8	8	383	350	390	2.56	405	2.47
8	0	383	330	370	2.70	385	2.60
4	4	1023	310	350	2.86	350	2.86
4	0	1023	290	330	3.03	330	3.03
4	4	383	230	270	3.70	270	3.70
4	0	383	210	250	4.00	250	4.00

5.2 Multiple Devices

5.2.1 I²C Interface Configuration for Multiple Devices

Multiple IQS9320 devices can be connected to a single I²C bus by selecting the I²C device address of each device with the state of the address select pins. The master device can sample all devices by sequentially addressing each device. The IQS9320 can be polled over I²C at any time.

Figure 5.1 shows an example configuration with four IQS9320 devices, each configured to use a different I²C address using the address select pins.

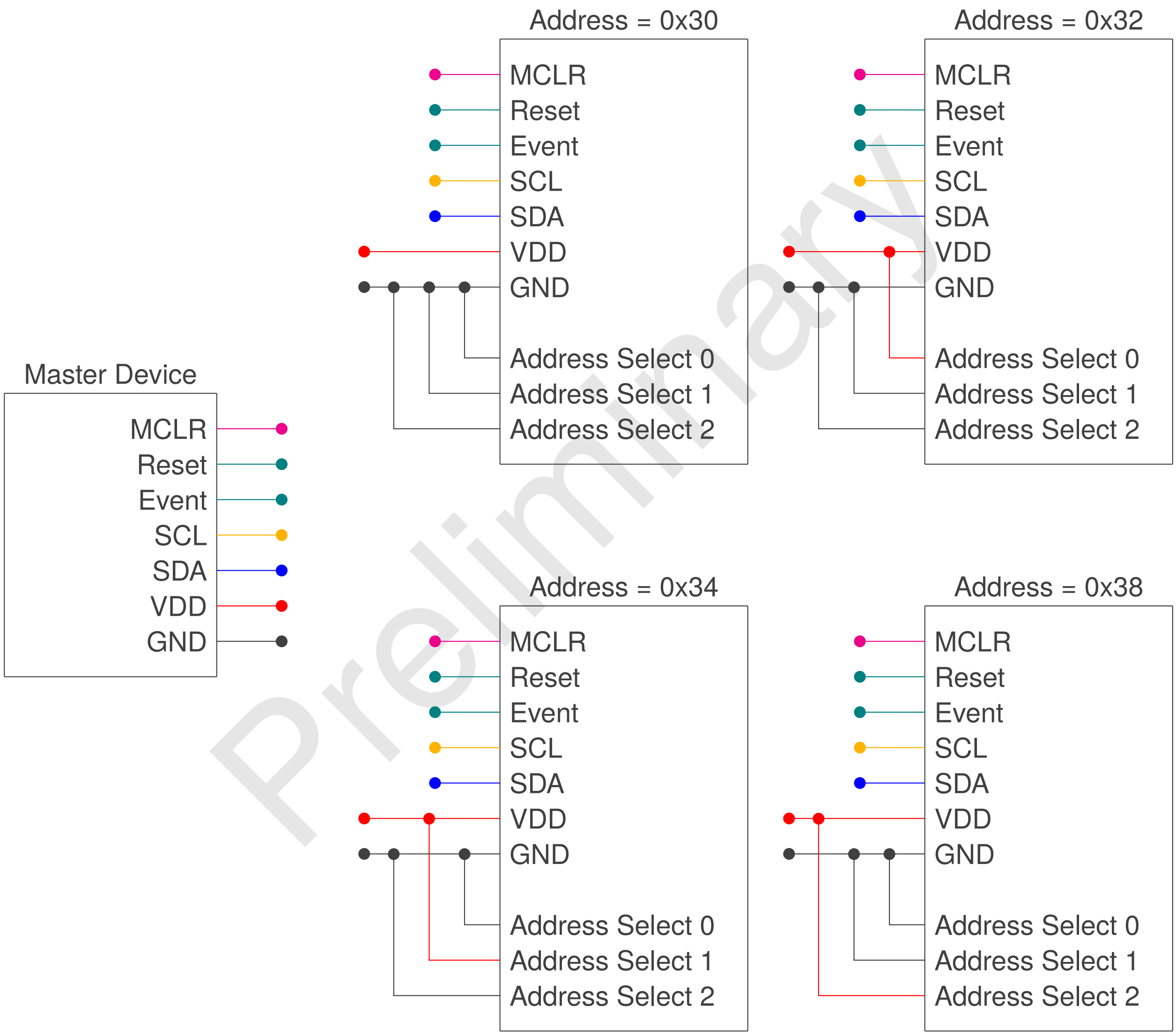


Figure 5.1: Multiple Devices with I²C Interface

The maximum sampling rate of a keyboard application is defined by the number of channels that are sampled by a single IQS9320 device. The number of channels per device defines the number of bytes that must be communicated over I²C per device to complete a sample. The time required to read a given number of bytes from a default read address (section 10.4.2) over an I²C connection with a clock speed of 1MHz is estimated as :

$$\text{Time per Device} = 20\mu s + \text{Bytes} \times 10\mu s \tag{1}$$

The time required to complete I²C communication per device determines the number of devices that can be sampled over a single I²C bus for a given sampling rate. A maximum of 8 IQS9320 devices can be connected to a single I²C peripheral.

Table 5.2: I²C Application Requirements

Number of Keys	Sample Type	Sample Rate [kHz]	Channels per Device	Bytes per Device	Time per Device [µs]	Number of Devices	Devices per I²C Peripheral	Number of I²C Peripherals
104	Activation Flags	1	20	3	50	6	8	1
104	Activation Flags	2	10	2	40	11	8	2
104	Activation Flags	3	6	1	30	18	8	3
104	Activation Flags	4	4	1	30	26	8	4
87	Activation Flags	1	20	3	50	5	8	1
87	Activation Flags	2	10	2	40	9	8	2
87	Activation Flags	3	6	1	30	15	8	2
87	Activation Flags	4	4	1	30	22	8	3
68	Activation Flags	1	20	3	50	4	8	1
68	Activation Flags	2	10	2	40	7	8	1
68	Activation Flags	3	6	1	30	12	8	2
68	Activation Flags	4	4	1	30	17	8	3
104	Normalised Delta	1	20	20	220	6	4	2
104	Normalised Delta	2	10	10	120	11	4	3
104	Normalised Delta	3	6	6	80	18	4	5
104	Normalised Delta	4	4	4	60	26	4	7
87	Normalised Delta	1	20	20	220	5	4	2
87	Normalised Delta	2	10	10	120	9	4	3
87	Normalised Delta	3	6	6	80	15	4	4
87	Normalised Delta	4	4	4	60	22	4	6
68	Normalised Delta	1	20	20	220	4	4	1
68	Normalised Delta	2	10	10	120	7	4	2
68	Normalised Delta	3	6	6	80	12	4	3
68	Normalised Delta	4	4	4	60	17	4	5

5.2.2 GPIO Interface Configuration for Multiple Devices

Multiple IQS9320 devices can be placed in a matrix where the channel states of all devices in a column can be sampled simultaneously. The master device will sequentially query each column and read the response of all devices in the column from the state of the row output pins.

Figure 5.2 shows an example layout with four IQS9320 devices arranged in a 2×2 device matrix.

All devices within the matrix share a single I^{2}C bus and have the same I^{2}C device address. I^{2}C communication can be enabled separately for each individual device by selecting a device using the row and column inputs.

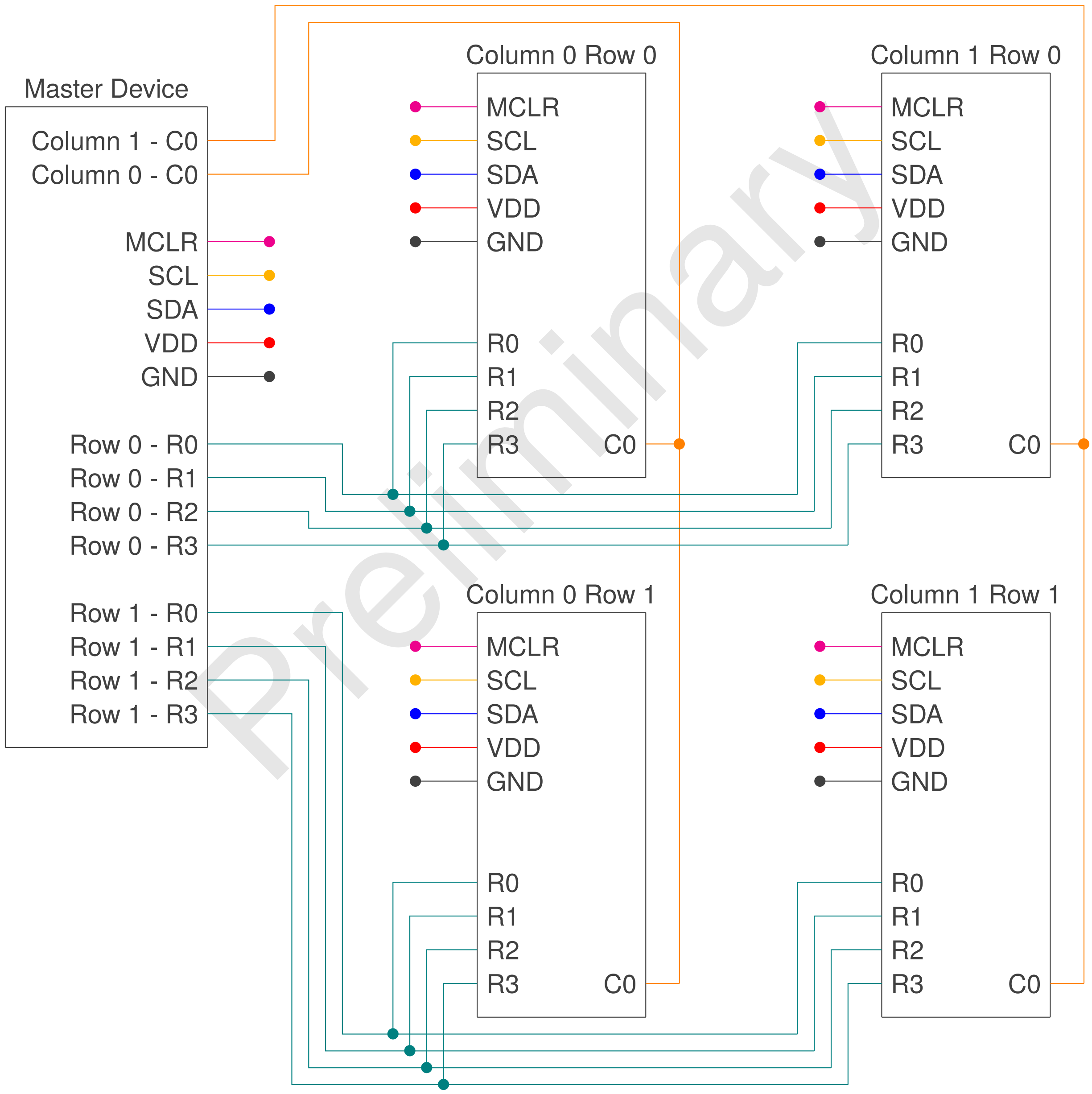


Figure 5.2: Multiple Devices with GPIO Interface

The maximum sampling rate of a keyboard application that uses the GPIO interface as the communication method to devices in a matrix is defined by the number of channels sampled per device. The time required to sample a single column is also defined by the number of channels sampled per device. The time required to sample a single column can be used to calculate the number of columns that can be sampled during a given sampling period.

$$\text{Maximum Columns} = \text{Floor}\left(\frac{\text{Sample Time}}{\text{Sample Time per Column}}\right) \tag{2}$$

The number of rows and columns can be selected such that the desired number of devices can be connected on the matrix and the number of columns does not exceed the limit calculated in Equation 2. The minimum number of GPIO pins required by the master device will be achieved by selecting a maximum number of columns and reducing the number of rows.

$$\text{Number of Devices} = \text{Columns} \times \text{Rows} \tag{3}$$

$$\text{GPIO Pins Required} = \text{Columns} + 4 \times \text{Rows} \tag{4}$$

Table 5.3 provides a summary of possible device matrix layouts that can be applied to popular keyboard layouts.

Table 5.3: Key Scan Application Requirements

Number of Keys	Sample Rate [kHz]	Channels per Device	Time per Column [µs]	Maximum Columns	Number of Devices	Columns	Rows	GPIO Pins Required
104	1	20	140	7	6	6	1	10
104	2	10	100	4	11	4	3	16
104	3	6	80	4	18	4	5	24
104	4	4	60	4	26	4	7	32
87	1	20	140	7	5	5	1	9
87	2	10	100	4	9	3	3	15
87	3	6	80	4	15	4	4	20
87	4	4	60	4	22	4	6	28
68	1	20	140	7	4	4	1	8
68	2	10	100	4	7	4	2	12
68	3	6	80	4	12	4	3	16
68	4	4	60	4	17	4	5	24

6 ProxFusion® Module

The IQS9320 ProxFusion® sensing architecture allows for up to 13 simultaneous inductive measurements with a total of up to 20 inductive channels that are sampled over 2 sampling cycles. The number of channels is defined by the sum of channels configured in the *Cycle 0 Channel Selection* and *Cycle 1 Channel Selection* registers.

The IQS9320 supports adjustable Rx and Tx pin selection for each channel. Table 6.1 lists the available Rx and Tx pin options with the associated value that must be written to the *Rx Pin Selection* and *Tx Pin Selection* registers.

Table 6.1: Rx and Tx Selection

Value	Pin Description	Selection	Value	Pin Description	Selection
0	CRx0A	Rx / Tx	23	CRx9A	Rx / Tx
1	CRx0B	Rx / Tx	24	CRx9B	Rx / Tx
2	CRx1A	Rx / Tx	25	CRx10A	Rx / Tx
3	CRx1B	Rx / Tx	26	CRx10B	Rx / Tx
4	CRx1C	Rx / Tx	27	CRx10C	Rx / Tx
5	CRx2A	Rx / Tx	28	CRx11A	Rx / Tx
6	CRx2B	Rx / Tx	29	CRx11B	Rx / Tx
7	CRx2C	Rx / Tx	30	CRx12A	Rx / Tx
8	CRx3A	Rx / Tx	31	CRx12B	Rx / Tx
9	CRx3B	Rx / Tx	32	-	-
10	CRx4A	Rx / Tx	33	CTx1	N/A
11	CRx4B	Rx / Tx	34	CTx2	N/A
12	CRx4C	Rx / Tx	35	CTx3	N/A
13	CRx5A	Rx / Tx	36	CTx4	N/A
14	CRx5B	Rx / Tx	37	CTx5	N/A
15	CRx6A	Rx / Tx	38	CTx6	Tx Only
16	CRx6B	Rx / Tx	39	CTx7	Tx Only
17	CRx6C	Rx / Tx	40	CTx8	Tx Only
18	CRx7A	Rx / Tx	41	CTx9	Tx Only
19	CRx7B	Rx / Tx	42	CTx10	Tx Only
20	CRx8A	Rx / Tx	43	CTx11	Tx Only
21	CRx8B	Rx / Tx	44	CTx12	Tx Only
22	CRx8C	Rx / Tx	45	CTx13	Tx Only

It is important to note that a single ProxFusion® sampling engine can only sample one input per sampling cycle. Therefore, 'CRx0A' and 'CRx0B' cannot be selected as Rx pins for channels sampled during the same cycle. Channel Rx and Tx pin selections must be configured such that a single sampling engine is used during both cycles to achieve a configuration supporting the maximum number of channels.

6.1 Counts

The sensing measurement of each channel returns a relative and unit-less value that is inversely proportional to inductance. This value is referred to as the *Raw Counts* value of a channel. All outputs are derived from *Raw Counts* values.

The maximum value of a *Raw Counts* sample can be defined in the *Hardware Settings* register. This will define a maximum analogue sampling time and may reduce the total sampling time of the device.

The *Linearised Counts* value is derived from the *Raw Counts* value of a channel with the equation below:

$$\textit{Linearised Counts} = \frac{3276750}{\textit{Raw Counts}} \tag{5}$$

A first-order low-pass IIR filter is applied to the *Linearised Counts* of each channel to reduce the high-frequency noise on the *Linearised Counts*. The response of this filter is defined by the *Linearised Counts Normal Power Beta* register when the device is in normal power mode. A higher beta parameter will result in a slower filter response and less noise on the channel.

6.2 Automatic Tuning Implementation (ATI)

The ATI of the IQS9320 allows the device to perform optimally with a wide range of external inductance values without the need to modify external components. The ATI is responsible for modifying the *Multiplier and Divider Selection* register of each channel to achieve a *Raw Counts* value equal to the value defined in the *ATI Target* register with some error.

The *ATI Band* register specifies the acceptable error from the *ATI Target*. If the ATI algorithm cannot achieve a *Raw Counts* value within the *ATI Band*, or the LTA of a channel drifts outside the valid range defined by the *ATI Band* the device will set the global *ATI Error Flag* in the *System Status* register and the channel-specific *ATI Error Flag* in the *Channel Data* register. The *System Configuration* register can be modified to disable the ATI or configure the device such that the device will automatically re-ATI when the *ATI Error Flag* is set.

$$(\textit{ATI Target} - \textit{ATI Band}) < \textit{Raw Count} < (\textit{ATI Target} + \textit{ATI Band}) \tag{6}$$

6.3 Reference Tracking (LTA)

The *Long-Term Average (LTA)* value of a channel is determined by applying a first-order low-pass IIR filter to the *Linearised Counts* value of a channel. The *LTA* is used to detect user interaction by providing a reference against which the *Linearised Counts* of a channel can be compared. The *LTA* of a channel should be configured to steadily track changes in the environment while ignoring input caused by user interaction.

6.3.1 Reference Halt

A *Reference Halt Flag* of a channel is set when the *Normalised Delta* value of a channel exceeds the *Reference Halt Threshold* and will result in the *LTA* value of the channel remaining constant such that user interactions will not affect the reference measurement. The *Reference Halt Flag* of each channel is available in the *Channel Data* register.

The *Reference Halt* event of each channel has a timeout period defined by the *Reference Halt Timeout* register, which can be adjusted in increments of 255 milliseconds. A reference halt timeout event will result in the device setting the *LTA* value of the relevant channel equal to the *Linearised Counts* value of the channel.

6.3.2 Fast Reference

The fast reference event will occur when the *Normalised Delta* value of a channel is less than the negative value defined in the *Fast Reference Threshold* register. The *Fast LTA Normal Power Beta* value will be selected as a filter parameter instead of the *LTA Normal Power Beta* filter parameter during a fast reference event if the device is in normal power mode. The *Fast LTA Normal Power Beta* filter parameter should always be less than the *LTA Normal Power Beta* filter parameter.

6.4 Delta

The difference between the *Linearised Counts* value and the *LTA* value of each channel is used to determine user interaction. This value is referred to as the *Delta* value of the channel and is available in the *Channel Data* register.

$$\textit{Delta} = \textit{LTA} - \textit{Linearised Counts} \tag{7}$$

6.5 Normalised Delta

The *Delta* value of each channel is normalised against an *Effective Max Delta* value that is adjustable for each channel. The *Normalised Delta* is expressed as an 8-bit fraction of the *Effective Max Delta*. The *Effective Max Delta* values compensate for the variance in sensitivity between inductive channels.

The *Normalised Delta* is used as the final output from which channel events are determined. The *Normalised Delta* values of all channels are compared to the *Activation Threshold*, *Reference Halt Threshold*, and *Fast Reference Threshold* values to set channel flags.

$$\textit{Normalised Delta} = \frac{255 \times \textit{Delta}}{\textit{Effective Max Delta}} \tag{8}$$

6.6 Channel Activation

Channel activation events occur when the *Normalised Delta* value of a channel exceeds the selected *Activation Threshold*. This results in the *Channel Activation Flag* being set. The channel activation event has no timeout period and will cause the channel to remain in activation indefinitely if no external input is given.

$$\textit{Normalised Delta} > \textit{Channel Activation Threshold} \tag{9}$$

The *Activation Threshold* of a channel is reduced by the value defined in the *Activation Hysteresis* register when the *Activation Flag* of the given channel is set. The original *Activation Threshold* is restored when the *Activation Flag* of the given channel is cleared.

$$\textit{Temporary Activation Threshold} = \text{Channel Activation Threshold} - \text{Activation Hysteresis} \tag{10}$$

The IQS9320 supports per-key activation threshold selection by setting the *Enable Individual Thresholds* bit in the *System Control* register. The activation threshold of each channel is then defined in the *Individual Activation Thresholds* register.

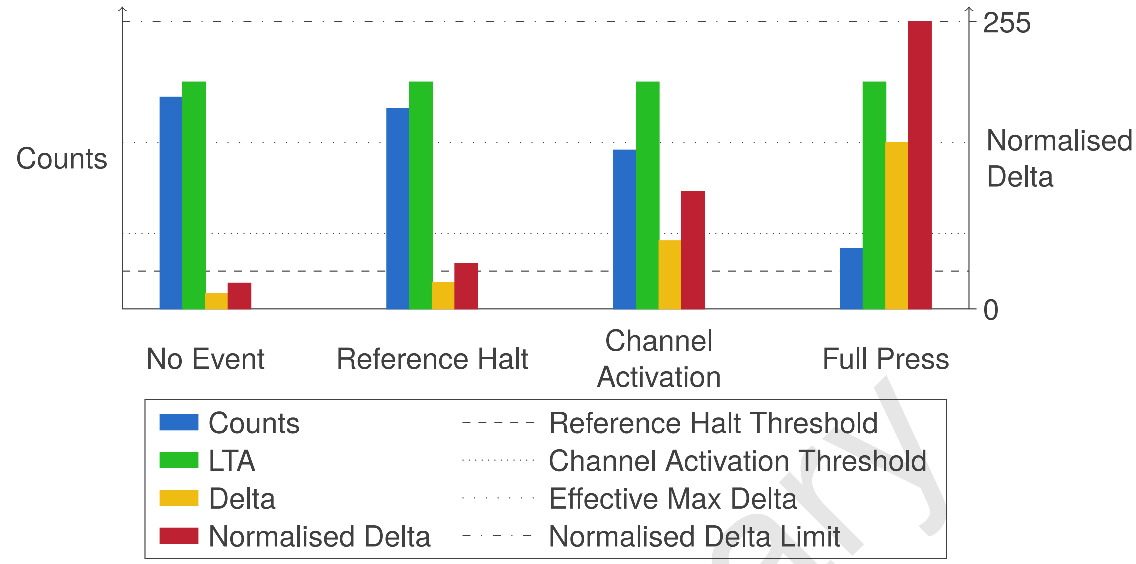


Figure 6.1: Channel Events

6.7 TriggerMax™

The TriggerMax™ dynamic actuation UI will track changes in the *Normalised Delta* value of channels for which the *Normalised Delta* exceeds the *Activation Threshold*. The *Movement* value is used to track changes in the *Normalised Delta* of a given channel. The *Movement Threshold* parameter defines the difference between the *Normalised Delta* value and the *Movement* value before a TriggerMax™ event can occur. A TriggerMax™ event may set or clear the *Channel Activation Flag* of a given channel and will set the *Movement* value equal to the *Normalised Delta* value. The behaviour of the TriggerMax™ UI is displayed in figure 6.2.

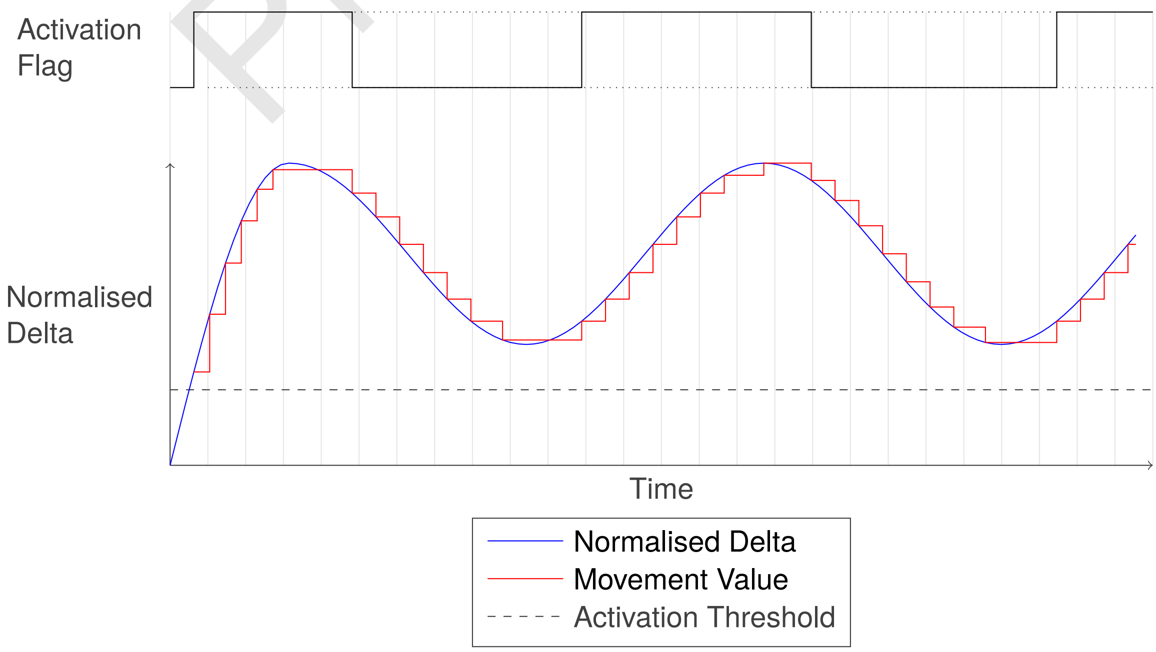


Figure 6.2: Movement Tracking Behaviour

7 GPIO Input Sequences

7.1 Key Scan

Key scanning can be used to read the *Channel Activation Flags* of all devices in a column simultaneously. The *Device Reset Flag* and *ATI Error Flag* states of each device in the column will also be produced as output. The key scanning state is entered with a falling edge produced by the master device if the *R0* and *R3* pins are *HIGH*. The master device will produce the *Device Reset Flag* and *ATI Error Flag* states on the first falling edge on *C0* and will continue to produce *Channel Activation Flag* states on alternating *C0* edges as indicated in figure 7.1. The number of *C0* edges required to complete the sequence is defined by the number of channels the device is configured for. All channel and device states are active when the associated row output is *LOW*.

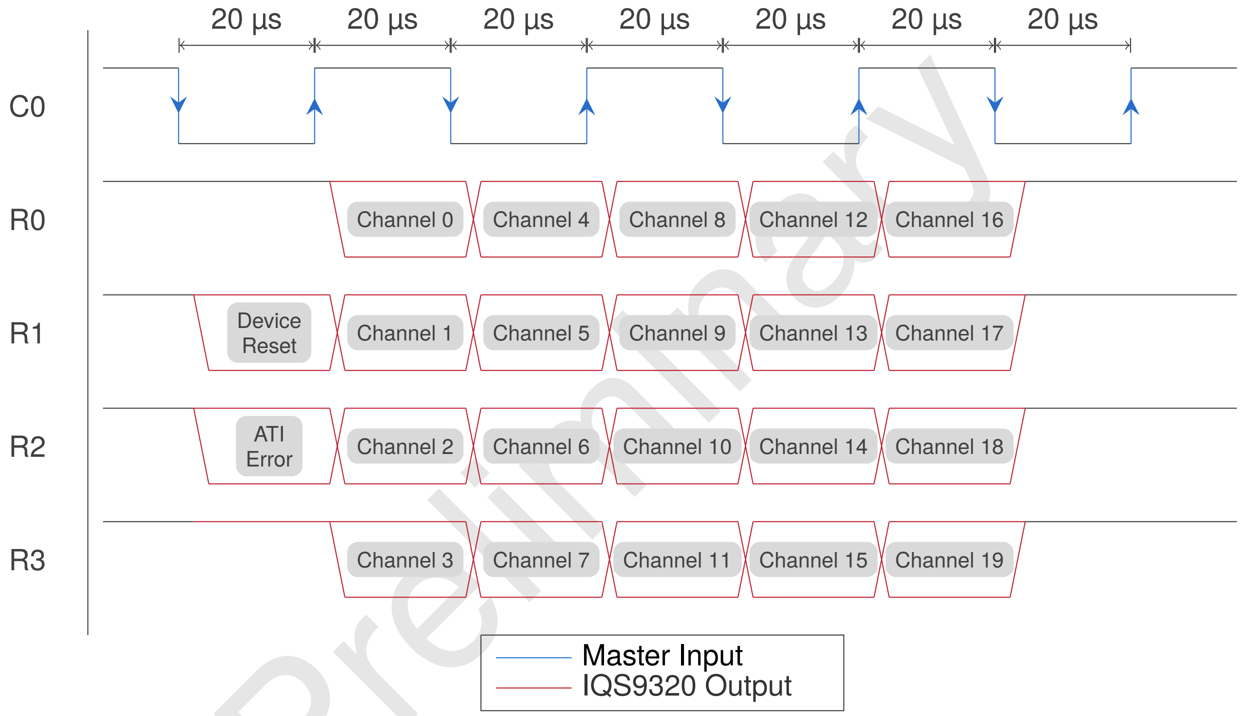


Figure 7.1: GPIO Sequence: Key Scan

7.2 I²C Configuration

The I²C peripheral of a single device in a matrix can be activated at a time for configuration purposes. All devices in the matrix have the same I²C device address and require input on the column and row pins to enable communication on the shared I²C bus.

The configuration state requires a falling edge on *C0*, with the *R0* pin *LOW* and the *R3* pin *HIGH*. The state is then entered with a rising edge on *C0*. The IQS9320 will then pull the *R0* pin *LOW* to indicate that the I²C peripheral is enabled. The *R0* pin will remain *LOW* until the master device exits the configuration state or when the configuration timeout event occurs. To stop other devices in the column from entering the configuration state, the master device must pull the *R3* pin *LOW* on selected devices. This behaviour is displayed in figure 7.2.

The *GPIO Sequence Configuration Timeout Period* register can be adjusted to select a timeout value between 1 and 255 milliseconds. The configuration timer is restarted when entering the configuration state, or when a valid I²C transaction occurs.

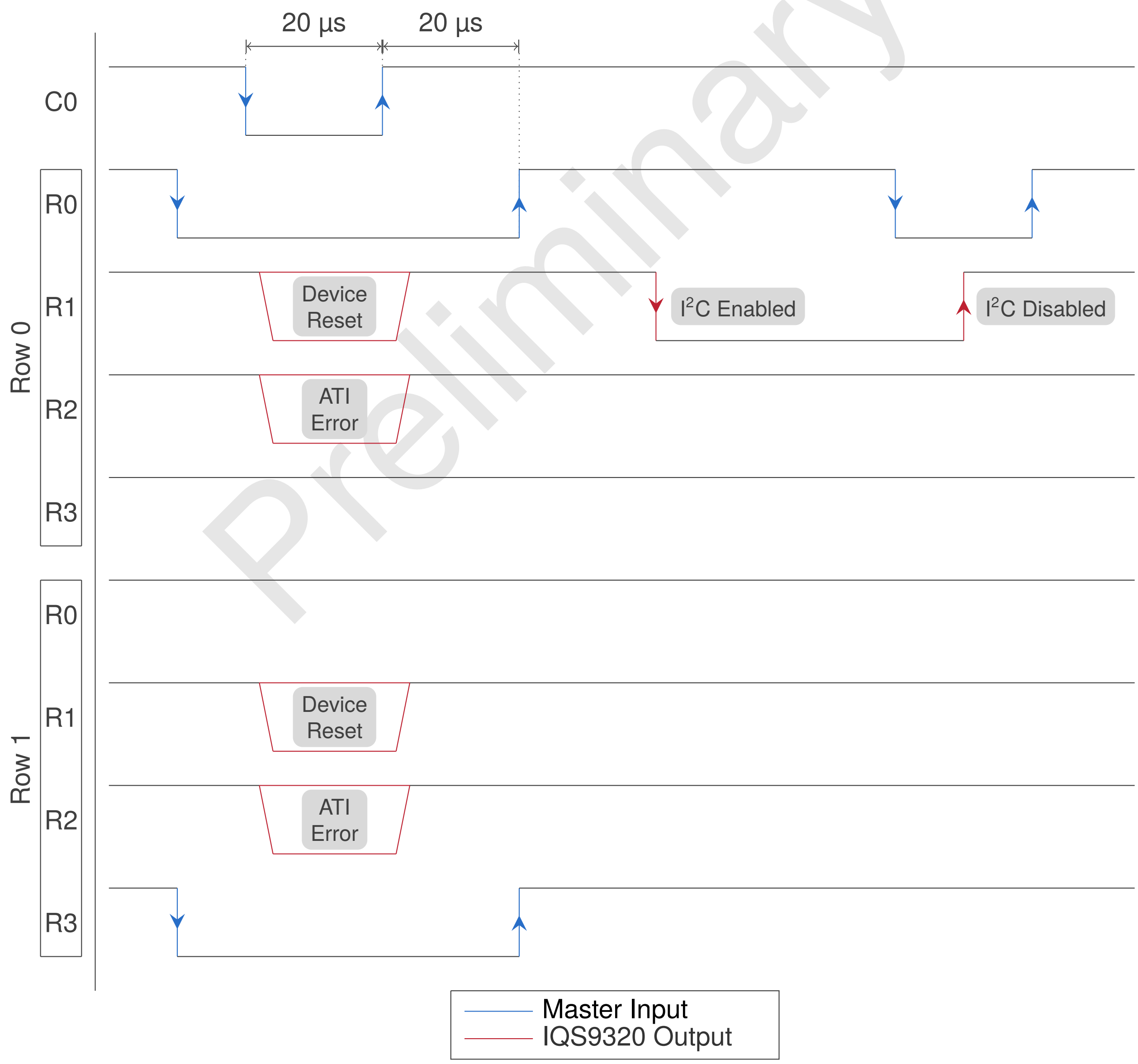


Figure 7.2: GPIO Sequence: I²C Configuration

7.3 Event/Standby Mode

The IQS9320 can enter a low-power state during which GPIO sequences are disabled. The device will either enter *Event Mode* or *Standby Mode* depending on the state of the *Enable Event Mode* bit in the *System Configuration* register. While in standby mode, the device will consume a minimal amount of power and will not complete any channel samples.

While in event mode, the device will sample channels at a rate defined by the *ULP Sample Interval* register. During *Event Mode*, the device will indicate channel activation events by pulling the *R1* pin (GPIO12) *LOW*. The *Event Mode* state will result in reduced power consumption when compared to the normal operating mode configured for the GPIO interface.

The event/standby mode sequence is started with a falling edge on the *C0* pin while the *R0* pin is *LOW* and the *R3* pin is *HIGH*. The state is then entered with a rising edge on the *R0* pin followed by a rising edge on the *C0* pin. The state is then exited with a valid I^{2}C transaction while the *C0* and *R0* pins are *LOW*. The *C0* and *R0* pins must be kept *LOW* for a minimum of 500µs after completing the I^{2}C transaction.

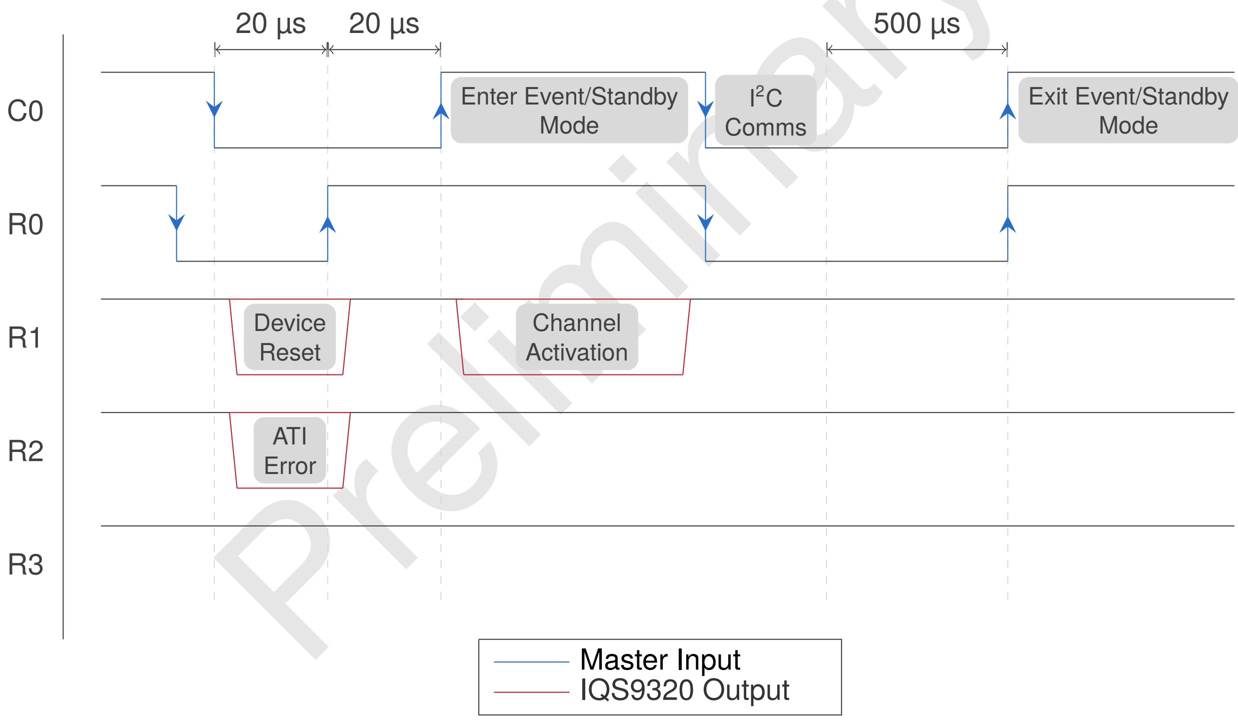


Figure 7.3: GPIO Sequence: Event/Standby

8 Power Modes

8.1 Mode Selection

The IQS9320 has 3 power mode selection options with an additional automatic power mode option for switching between power modes without the need for commands from a master device. The power mode can be selected in the *System Control* register.

- Normal Power
- Low Power
- Ultra-Low Power
- Automatic Power Modes

8.2 Mode Parameters

The IQS9320 has 2 power mode parameters that define the sample rate, current consumption, and automatic power mode behaviour.

- Sample Interval
- Mode Timeout

The sample interval parameter defines in milliseconds the period between samples and is responsible for the resulting current consumption of the device. It is recommended to configure the IQS9320 such that the sample interval increases as a lower power mode is selected.

Given that the automatic power mode is selected, the mode timeout parameter defines in milliseconds the period for which the device will remain in a given power mode before a lower mode is automatically selected.

8.3 Automatic Power Modes

The automatic power mode of the device will cause the device to lower the active power mode when no wake-up event occurs during the period defined by the *Mode Timeout* parameter of the active power mode. The device may enter the 'Ultra-Low Power' mode where it will remain until a wake-up event occurs or the master device modifies the power mode selection.

A wake-up event can be caused by a channel activation or I²C event and will result in the device returning to the 'Normal Power Mode' where it will remain for the duration of the *Normal Power Mode Timeout* if no other wake-up event occurs. The active wake-up events can be modified in the *System Configuration* register.

8.4 Standby Mode

The IQS9320 supports a standby mode that can be entered by setting the *Standby Mode* bit in the *System Control* register or by executing the associated GPIO input sequence. No analogue sampling or digital processing occurs while the device is in standby mode, resulting in very low current consumption. The device will respond to I²C instructions such that the *System Control* register can be modified and the device can exit standby mode.

9 Additional Features

9.1 Reset Indication

At startup, or after a reset, the reset flag will be set in the *System Status* register. The master device can acknowledge the reset by setting the *Acknowledge Reset* bit in the *System Control* register. If the *Reset Flag* bit is set again after being acknowledged, the master device will know a reset has occurred and can act accordingly.

The master device can reset the IQS9320 by setting the *Software Reset* bit in the *System Control* register or by pulling the *MCLR* pin *LOW* as described in section 4.5.

The *Enable Reset Pin* bit in the *System Configuration* register is used to configure the reset pin, GPIO13, as an open-drain active-low output to indicate that the *Reset Flag* is set in the *System Status* register.

9.2 Event Pin

The *Enable Event Pin* bit in the *System Configuration* register is used to configure the event pin, GPIO14, as an open-drain active-low output to indicate that the *Activation Flag* has been set in the *System Status* register.

This will allow the IQS9320 device to communicate user interaction to the master device with minimal delay and no action required from the master device.

9.3 Automatic Calibration

The IQS9320 supports an automatic calibration procedure wherein the effects of a metal target moving relative to the inductive sensing coil are emulated by adjusting the Tx frequency of the coil. The calibration procedure will estimate a *Max Delta* value for each channel such that the full range of a key press can be expressed by the *Normalised Delta* value of the channel.

The *Calibration Step* parameter in the *Calibration Parameters* register defines the amount the Tx frequency is adjusted by. The frequency adjustment is in steps of approximately 0.4MHz.

The calibration procedure returns a *Calibration Counts* value for each channel, which is the *Counts* value sampled when the Tx frequency is affected by the *Calibration Step* parameter. The *Calibration Counts* value is then scaled by the *Calibration Correction* parameter to get a better estimation of the *Max Delta* value. The *Calibration Max Delta* is then estimated by calculating the difference between the *Counts* value sampled during and after the change in frequency as displayed in Equation 11.

$$\text{Calibration Max Delta} = \text{Linearised Counts} - \frac{\text{Calibration Counts} \times \text{Calibration Correction}}{127} \tag{11}$$

For more information regarding the automatic calibration procedure refer to Section C.1.

9.4 Manual Calibration

The *Sampled Max Delta* register tracks the largest *Delta* values observed by each channel when the *Sample Max Counts* bit is set in the *System Control* register.

The *Sampled Max Delta* value is used to express the total travel range of a key after that key has been fully pressed. The *Sampled Max Delta* value can then be written to the *Effective Max Delta* register, such that the *Normalised Delta* value of a channel will express the full range of the key press.

For more information regarding the manual calibration procedure refer to Section C.2.

9.5 External Clock Input

The IQS9320 can be configured to use an external clock input for the ProxFusion® modules by setting the *Enable External POSC Clock Source* bit in the *System Configuration* register. The clock source should be provided as a square wave with a 50% duty cycle, peak-to-peak voltage of 3.3V, DC offset voltage of 1.65V, and a maximum frequency of 16MHz.

The *External Clock Active* bit in the *System Status* register will be set when the system is actively using the external clock. The device will not use the external clock source if any channel Tx pins are configured as CTx12 or CTx13.

The *External POSC Clock Output* pin (CTx12) will be *HIGH* when the clock source must be active.

10 I²C Interface

10.1 Module Specification

The device supports a standard two-wire I²C interface with a maximum bit rate of up to 1Mbps. The memory structures accessible over the I²C interface are byte-addressable with 16-bit address values. 16-bit or 32-bit values are packed with little-endian byte order and are stored in word-aligned addresses.

- Standard two-wire interface
- *Fast-Mode Plus* I²C with up to 1Mbps bit rate
- 7-bit device address
- 16-bit register address
- Little-endian

The master device may use the I²C interface to read or write data at any time. The device will exit a sleep condition when I²C transactions occur while the device is in a low-power mode and may be configured to return to normal power when automatic power modes are enabled.

10.2 I²C Address Options

The IQS9320 supports 8 different 7-bit device address options which can be selected by setting the state of the 3 address selection pins. The default device address options are listed in Table 10.1.

Table 10.1: I²C addressing options

Address Select 2	Address Select 1	Address Select 0	7-bit Device Address	8-bit Read Address	8-bit Write Address
LOW	LOW	LOW	0x30	0x61	0x60
LOW	LOW	HIGH	0x32	0x65	0x64
LOW	HIGH	LOW	0x34	0x69	0x68
LOW	HIGH	HIGH	0x36	0x6D	0x6C
HIGH	LOW	LOW	0x38	0x71	0x70
HIGH	LOW	HIGH	0x3A	0x75	0x74
HIGH	HIGH	LOW	0x3C	0x79	0x78
HIGH	HIGH	HIGH	0x3E	0x7D	0x7C

10.3 Memory Management

The IQS9320 can be addressed and configured over I²C at any time and therefore requires 2 configuration memory structures. One structure is actively used for sampling and processing channel data, while the other is always available to a master device via the I²C peripheral. The modifications made to the memory structure available over I²C will not affect the sampling and processing of channel data until the *Reconfigure Device* bit has been set in the *System Control* register.

This affects all read/write registers excluding the *System Control* register which is monitored after each cycle. The read-only registers will always contain the latest data available to the device.

10.4 Read and Write Operations

10.4.1 I²C Read From Specific Address

The read operation is displayed in Figure 10.1. The master will first provide a start condition followed by the device address with a write command. The IQS9320 will respond with an acknowledgement after which the master device will transmit two bytes defining the register address. The master will then send a repeated start condition followed by the device address with a read command. The IQS9320 will then transmit data from the requested address and will continue to do so while the master acknowledges each byte. The read operation is ended when the master does not acknowledge the last byte received and produces a stop condition.

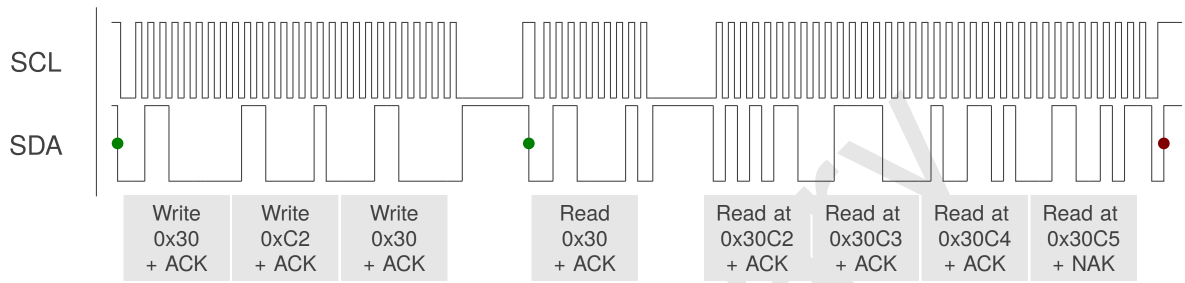


Figure 10.1: I2C read example

10.4.2 I²C Read From Default Address

A default address can be defined such that no write operation is required prior to reading data from the IQS9320. The master will first provide a start condition followed by the device address with a read command. The IQS9320 will respond with an acknowledgement followed by the first byte of data read from the default address. The IQS9320 will continue to transmit data from the initial default read address while the master acknowledges each byte. The read operation is ended when the master does not acknowledge the last byte received and produces a stop condition. This operation is displayed in Figure 10.2.

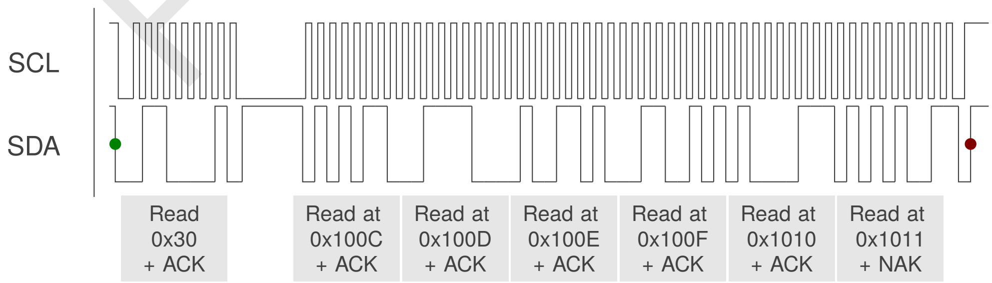


Figure 10.2: I2C read default address example

10.4.3 I²C Write To Specific Address

The write operation is displayed in Figure 10.3. The master will first provide a start condition followed by the device address with a write command. The IQS9320 will respond with an acknowledgement after which the master device will transmit two bytes defining the register address. The slave acknowledges the register address bytes. The master may then write a series of bytes to the register address and the addresses which follow, with each byte being acknowledged by the slave. The write operation is ended when the master produces a stop condition.

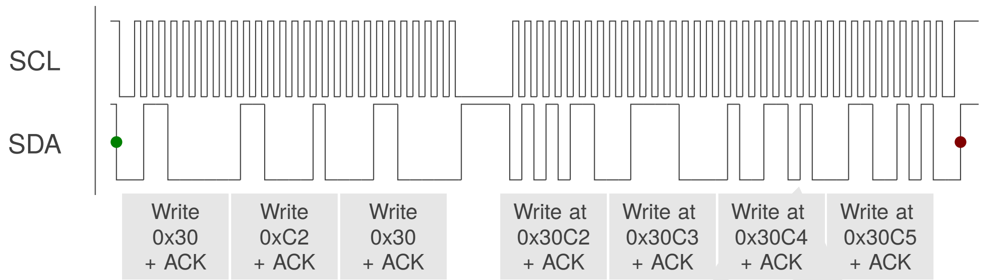


Figure 10.3: I2C write example

11 Ordering Information

11.1 Ordering Code

IQS9320 zzz ppb

Table 11.1: Ordering Code Description

Description	Placeholder	Options	
		Value	Description
Configuration	zzz	000	20-key Configuration I^2C Interface I^2C Address Range = 0x30-0x3E
		001	20-key Configuration GPIO Interface
Package Type	pp	QF	QFN-52 Package
Bulk Packaging	b	R	QFN-52 Reel (3000pcs/reel)

Example : IQS9320-000QFR

11.2 QFN52 Top Markings

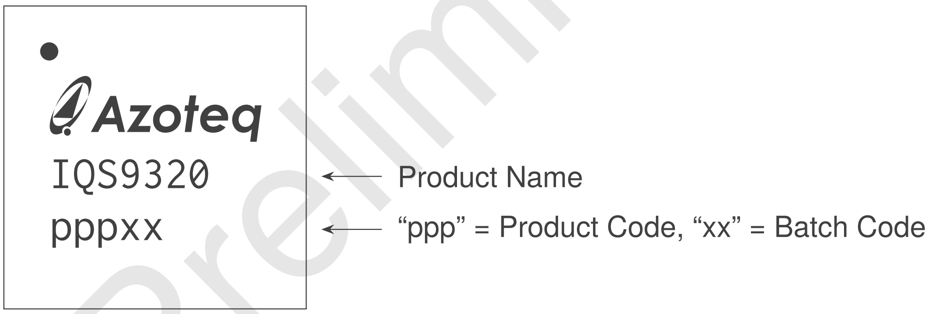


Figure 11.1: IQS9320-QFN52 Package Top Marking

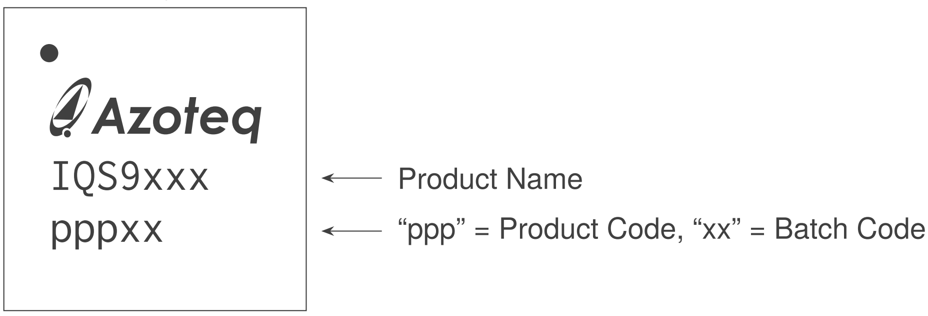


Figure 11.2: QFN52 Generic Package Top Marking

12 QFN52 Package Information

12.1 QFN52 Package Outline

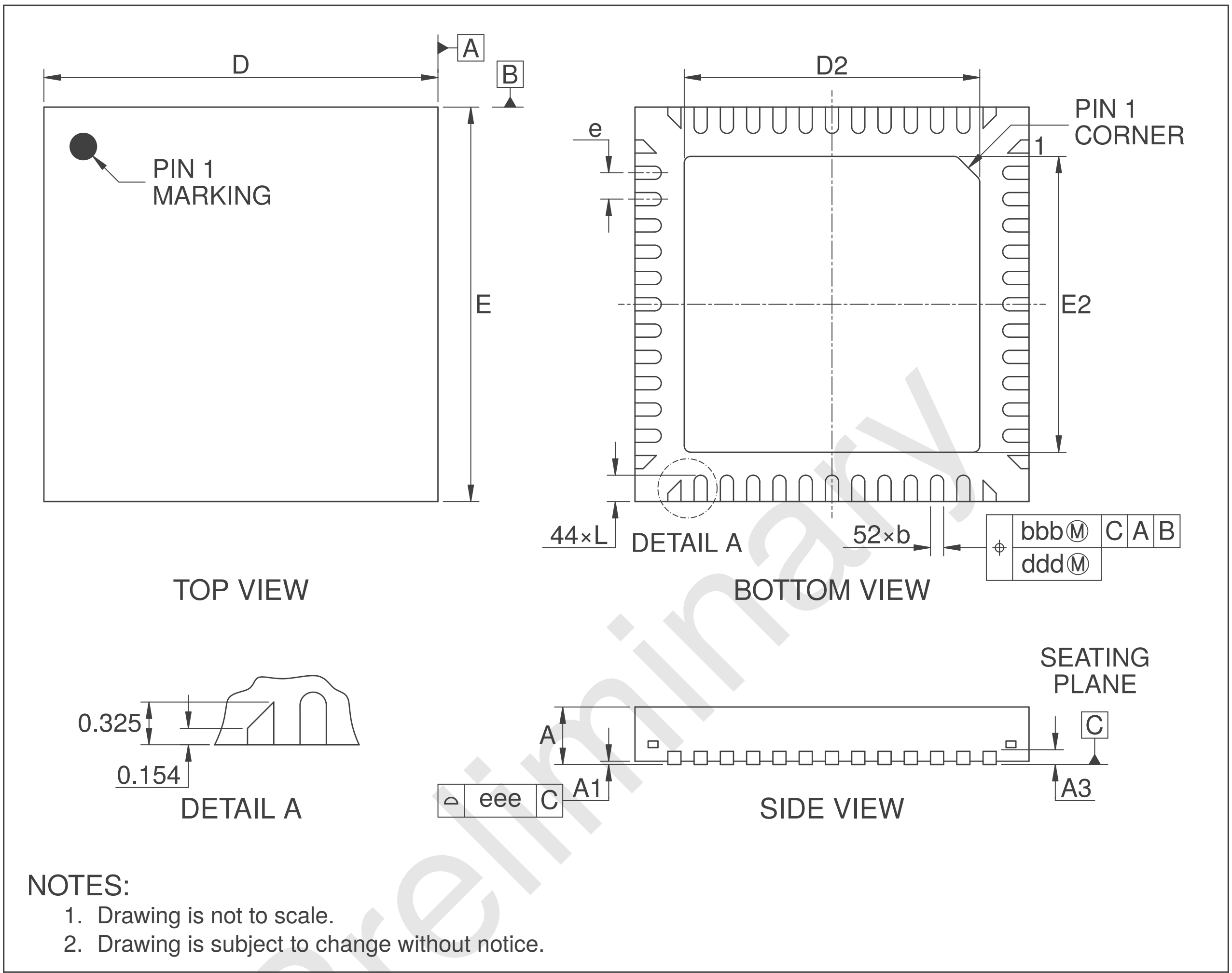


Figure 12.1: QFN52 Package Outline Visual Description

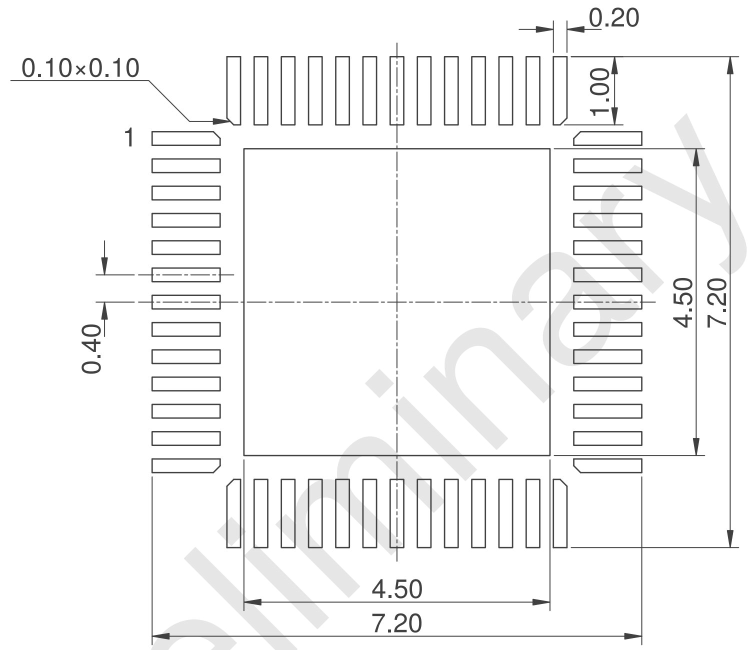
Table 12.1: QFN52 Package Dimensions [mm]

Dimension	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
D	6.00 BSC		
E	6.00 BSC		
D2	4.40	4.50	4.60
E2	4.40	4.50	4.60
b	0.15	0.20	0.25
e	0.40 BSC		
L	0.35	0.40	0.45

Table 12.2: QFN52 Package Tolerances [mm]

Tolerance	Millimeters
bbb	0.10
ddd	0.05
eee	0.08

12.2 QFN52 Recommended Footprint



RECOMMENDED FOOTPRINT

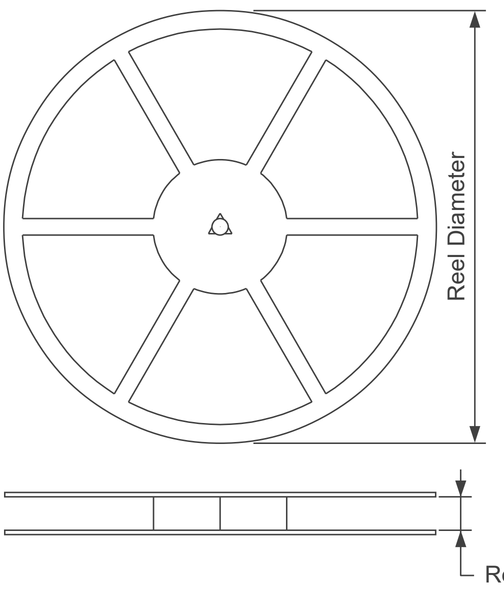
NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.

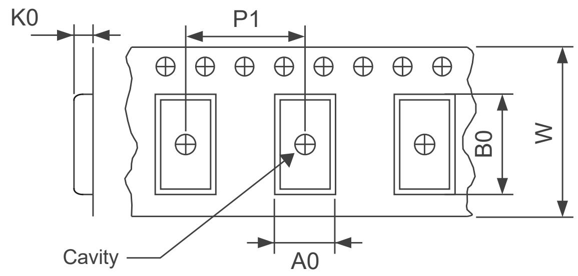
Figure 12.2: QFN52 Recommended Footprint

12.3 Tape and Reel Specifications

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

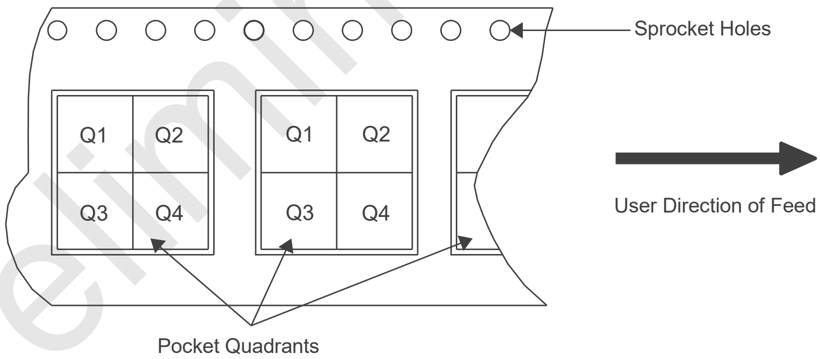


Figure 12.3: Tape and Reel Specification

Table 12.3: Tape and Reel Specifications

Package Type	Pins	Dimension [Millimeters]							Pin 1 Quadrant
		Reel Diameter	Reel Width	A0	B0	K0	P1	W	
QFN52	52	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

13 I²C Memory Map

Address	Length	Description	Default	Notes
Read Only		**Version Information**		
0x0000	2	Product Number	0x0716	
0x0002	2	Product Major Version	0x0001	
0x0004	2	Product Minor Version	0x0000	
0x0006	4	Product SHA	-	
0x000A	2	Library Number	0x037D	
0x000C	2	Library Major Version	0x0001	
0x000E	2	Library Minor Version	0x0000	
0x0010	4	Library SHA	-	
0x0014	6	Unique Identifier	-	
Read Only		**Device Data**		
0x1000	2	System Status	0x0040	Table A.1
0x1002	4	ATI Error Flags	-	Table A.2
0x1006	4	Reference Halt Flags	-	Table A.3
0x100A	4	Activation Flags	-	Table A.4
0x100E	20	Normalised Delta	-	uint8 [20]
0x1022	20	Movement	-	uint8 [20]
0x1036	40	Delta	-	int16 [20]
0x105E	40	Counts	-	uint16 [20]
0x1086	40	LTA	-	uint16 [20]
0x10AE	40	Raw Counts	-	uint16 [20]
Read-Write		**Device Configuration**		
0x2000	2	System Control	0x0000	Table A.5
0x2002	2	System Configuration	0x3E2B	Table A.6
0x2004	2	Normal Power Sampling Interval	0x0000	ms
0x2006	2	Normal Power Timeout	0x1388	ms
0x2008	2	Low Power Sampling Interval	0x0028	ms
0x200A	2	Low Power Timeout	0x1388	ms
0x200C	2	Ultra-Low Power Sampling Interval	0x0050	ms
0x200C	2	Ultra-Low Power Timeout	0x0000	ms
0x2010	2	Default Read Location	0x100A	
0x2012	1	GPIO Sequence Timeout Period	0x0A	ms
0x2013	1	GPIO Sequence Configuration Timeout Period	0x14	ms
0x2014	2	I²C Transaction Timeout Period	0x00C8	ms
Read-Write		**Channel Configuration**		
0x3000	40	Multiplier and Divider Parameters	0x4E77	Table A.7
0x3028	40	Calibration Parameters	0x0000	Table A.8
0x3050	40	Effective Max Delta	0x2710	uint16 [20]
0x3078	40	Sampled Max Delta	0x0000	uint16 [20]
0x30A0	40	Calibration Max Delta	0x0000	uint16 [20]
0x30C8	40	Calibration Counts	0x0000	uint16 [20]
0x30F0	20	Individual Activation Thresholds	0x28	uint8 [20]

Continued on next page

0x3104	1	Cycle 0 Channel Selection	0x0A	Section 6
0x3105	1	Cycle 1 Channel Selection	0x0A	Section 6
0x3106	4	Channel Disable	0x00000000	Table A.9
0x310A	20	Rx Pin Selection	-	uint8 [20]
0x311E	20	Tx Pin Selection	-	uint8 [20]
0x3132	2	ATI Target	0x00C8	
0x3134	2	ATI Band	0x0032	
0x3136	1	Activation Threshold	0x28	
0x3137	1	Reference Halt Threshold	0x14	
0x3138	1	Fast Reference Threshold	0x0A	
0x3139	1	Movement Threshold	0x08	
0x313A	1	LTA Normal Power Beta	0x0A	
0x313B	1	LTA Low Power Beta	0x06	
0x313C	1	LTA Ultra-Low Power Beta	0x05	
0x313D	1	Fast LTA Normal Power Beta	0x08	
0x313E	1	Fast LTA Low Power Beta	0x05	
0x313F	1	Fast LTA Ultra-Low Power Beta	0x04	
0x3140	1	Linearised Counts Normal Power Beta	0x02	
0x3141	1	Linearised Counts Low Power Beta	0x01	
0x3142	1	Linearised Counts Ultra-Low Power Beta	0x00	
0x3144	1	Reference Halt Timeout Value	0x08	256ms
0x3145	1	Activation Hysteresis	0x05	
0x3146	2	Timing Generator Settings	0x00	Table A.10
0x3148	2	Hardware Settings	0x012C	Table A.11

A Memory Map Descriptions

A.1 System Status (0x1000)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							
Default	0							

Bit	7	6	5	4	3	2	1	0
Description	External Clock Active	Reset Flag	Reference Halt	Activation	ATI Active	ATI Error	Power Mode Selection	
Default	0	1	0	0	0	0	0	

- Bit 0-1: **Power Mode Flag**
  - 0: Normal Power
  - 1: Low Power
  - 2: Ultra-Low Power
- Bit 2: **ATI Error Flag**
  - 0: All channels are within ATI Band
  - 1: One or more channels are outside ATI Band
- Bit 3: **ATI Active Flag**
  - 0: No channels are executing ATI sequence
  - 1: One or more channels are executing ATI sequence
- Bit 4: **Activation Flag**
  - 0: No channels within their activation threshold
  - 1: One or more channels are within their activation threshold
- Bit 5: **Reference Halt Flag**
  - 0: No channels are within the reference halt threshold
  - 1: One or more channels are within the reference halt threshold
- Bit 6: **Reset Flag**
  - 0: Reset has been acknowledged
  - 1: Reset has occurred and has not been acknowledged
- Bit 7: **External Clock Active**
  - 0: The internal POSC oscillator is used as input for the ProxEngines
  - 1: An external clock is used as input for the ProxEngines

A.2 ATI Error Flags (0x1002)

Bit	31	30	29	28	27	26	25	24
Description	Reserved							
Default	0							

Bit	23	22	21	20	19	18	17	16
Description	Reserved				CH19 ATI Error Flag	CH18 ATI Error Flag	CH17 ATI Error Flag	CH16 ATI Error Flag
Default	0				0	0	0	0

Bit	15	14	13	12	11	10	9	8
Description	CH15 ATI Error Flag	CH14 ATI Error Flag	CH13 ATI Error Flag	CH12 ATI Error Flag	CH11 ATI Error Flag	CH10 ATI Error Flag	CH9 ATI Error Flag	CH8 ATI Error Flag
Default	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Description	CH7 ATI Error Flag	CH6 ATI Error Flag	CH5 ATI Error Flag	CH4 ATI Error Flag	CH3 ATI Error Flag	CH2 ATI Error Flag	CH1 ATI Error Flag	CH0 ATI Error Flag
Default	0	0	0	0	0	0	0	0

- Bit 0: **CH0 ATI Error Flag**
  - 0: CH0 Counts within ATI Band
  - 1: CH0 Counts outside ATI Band
- Bit 1: **CH1 ATI Error Flag**
  - 0: CH1 Counts within ATI Band
  - 1: CH1 Counts outside ATI Band
- Bit 2: **CH2 ATI Error Flag**
  - 0: CH2 Counts within ATI Band
  - 1: CH2 Counts outside ATI Band
- Bit 3: **CH3 ATI Error Flag**
  - 0: CH3 Counts within ATI Band
  - 1: CH3 Counts outside ATI Band
- Bit 4: **CH4 ATI Error Flag**
  - 0: CH4 Counts within ATI Band
  - 1: CH4 Counts outside ATI Band
- Bit 5: **CH5 ATI Error Flag**
  - 0: CH5 Counts within ATI Band
  - 1: CH5 Counts outside ATI Band
- Bit 6: **CH6 ATI Error Flag**
  - 0: CH6 Counts within ATI Band
  - 1: CH6 Counts outside ATI Band
- Bit 7: **CH7 ATI Error Flag**
  - 0: CH7 Counts within ATI Band
  - 1: CH7 Counts outside ATI Band
- Bit 8: **CH8 ATI Error Flag**
  - 0: CH8 Counts within ATI Band
  - 1: CH8 Counts outside ATI Band
- Bit 9: **CH9 ATI Error Flag**
  - 0: CH9 Counts within ATI Band
  - 1: CH9 Counts outside ATI Band
- Bit 10: **C1H0 ATI Error Flag**
  - 0: CH10 Counts within ATI Band
  - 1: CH10 Counts outside ATI Band
- Bit 11: **CH11 ATI Error Flag**
  - 0: CH11 Counts within ATI Band

- 1: CH11 Counts outside ATI Band

- Bit 12: **CH12 ATI Error Flag**
  - 0: CH12 Counts within ATI Band
  - 1: CH12 Counts outside ATI Band
- Bit 13: **CH13 ATI Error Flag**
  - 0: CH13 Counts within ATI Band
  - 1: CH13 Counts outside ATI Band
- Bit 14: **CH14 ATI Error Flag**
  - 0: CH14 Counts within ATI Band
  - 1: CH14 Counts outside ATI Band
- Bit 15: **CH15 ATI Error Flag**
  - 0: CH15 Counts within ATI Band
  - 1: CH15 Counts outside ATI Band
- Bit 16: **CH16 ATI Error Flag**
  - 0: CH16 Counts within ATI Band
  - 1: CH16 Counts outside ATI Band
- Bit 17: **CH17 ATI Error Flag**
  - 0: CH17 Counts within ATI Band
  - 1: CH17 Counts outside ATI Band
- Bit 18: **CH18 ATI Error Flag**
  - 0: CH18 Counts within ATI Band
  - 1: CH18 Counts outside ATI Band
- Bit 19: **CH19 ATI Error Flag**
  - 0: CH19 Counts within ATI Band
  - 1: CH19 Counts outside ATI Band

A.3 Reference Halt Flags (0x1006)

Bit	31	30	29	28	27	26	25	24
Description	Reserved							
Default	0							

Bit	23	22	21	20	19	18	17	16
Description	Reserved				CH19 Ref Halt Flag	CH18 Ref Halt Flag	CH17 Ref Halt Flag	CH16 Ref Halt Flag
Default	0				0	0	0	0

Bit	15	14	13	12	11	10	9	8
Description	CH15 Ref Halt Flag	CH14 Ref Halt Flag	CH13 Ref Halt Flag	CH12 Ref Halt Flag	CH11 Ref Halt Flag	CH10 Ref Halt Flag	CH9 Ref Halt Flag	CH8 Ref Halt Flag
Default	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Description	CH7 Ref Halt Flag	CH6 Ref Halt Flag	CH5 Ref Halt Flag	CH4 Ref Halt Flag	CH3 Ref Halt Flag	CH2 Ref Halt Flag	CH1 Ref Halt Flag	CH0 Ref Halt Flag
Default	0	0	0	0	0	0	0	0

- Bit 0: **CH0 Reference Halt Flag**
  - 0: CH0 Normalised Delta less than Reference Halt Threshold
  - 1: CH0 Normalised Delta greater than Reference Halt Threshold
- Bit 1: **CH1 Reference Halt Flag**
  - 0: CH1 Normalised Delta less than Reference Halt Threshold
  - 1: CH1 Normalised Delta greater than Reference Halt Threshold
- Bit 2: **CH2 Reference Halt Flag**
  - 0: CH2 Normalised Delta less than Reference Halt Threshold
  - 1: CH2 Normalised Delta greater than Reference Halt Threshold
- Bit 3: **CH3 Reference Halt Flag**
  - 0: CH3 Normalised Delta less than Reference Halt Threshold

- 1: CH3 Normalised Delta greater than Reference Halt Threshold

- Bit 4: **CH4 Reference Halt Flag**
  - 0: CH4 Normalised Delta less than Reference Halt Threshold
  - 1: CH4 Normalised Delta greater than Reference Halt Threshold
- Bit 5: **CH5 Reference Halt Flag**
  - 0: CH5 Normalised Delta less than Reference Halt Threshold
  - 1: CH5 Normalised Delta greater than Reference Halt Threshold
- Bit 6: **CH6 Reference Halt Flag**
  - 0: CH6 Normalised Delta less than Reference Halt Threshold
  - 1: CH6 Normalised Delta greater than Reference Halt Threshold
- Bit 7: **CH7 Reference Halt Flag**
  - 0: CH7 Normalised Delta less than Reference Halt Threshold
  - 1: CH7 Normalised Delta greater than Reference Halt Threshold
- Bit 8: **CH8 Reference Halt Flag**
  - 0: CH8 Normalised Delta less than Reference Halt Threshold
  - 1: CH8 Normalised Delta greater than Reference Halt Threshold
- Bit 9: **CH9 Reference Halt Flag**
  - 0: CH9 Normalised Delta less than Reference Halt Threshold
  - 1: CH9 Normalised Delta greater than Reference Halt Threshold
- Bit 10: **C1H0 Reference Halt Flag**
  - 0: CH10 Normalised Delta less than Reference Halt Threshold
  - 1: CH10 Normalised Delta greater than Reference Halt Threshold
- Bit 11: **CH11 Reference Halt Flag**
  - 0: CH11 Normalised Delta less than Reference Halt Threshold
  - 1: CH11 Normalised Delta greater than Reference Halt Threshold
- Bit 12: **CH12 Reference Halt Flag**
  - 0: CH12 Normalised Delta less than Reference Halt Threshold
  - 1: CH12 Normalised Delta greater than Reference Halt Threshold
- Bit 13: **CH13 Reference Halt Flag**
  - 0: CH13 Normalised Delta less than Reference Halt Threshold
  - 1: CH13 Normalised Delta greater than Reference Halt Threshold
- Bit 14: **CH14 Reference Halt Flag**
  - 0: CH14 Normalised Delta less than Reference Halt Threshold
  - 1: CH14 Normalised Delta greater than Reference Halt Threshold
- Bit 15: **CH15 Reference Halt Flag**
  - 0: CH15 Normalised Delta less than Reference Halt Threshold
  - 1: CH15 Normalised Delta greater than Reference Halt Threshold
- Bit 16: **CH16 Reference Halt Flag**
  - 0: CH16 Normalised Delta less than Reference Halt Threshold
  - 1: CH16 Normalised Delta greater than Reference Halt Threshold
- Bit 17: **CH17 Reference Halt Flag**
  - 0: CH17 Normalised Delta less than Reference Halt Threshold
  - 1: CH17 Normalised Delta greater than Reference Halt Threshold
- Bit 18: **CH18 Reference Halt Flag**
  - 0: CH18 Normalised Delta less than Reference Halt Threshold
  - 1: CH18 Normalised Delta greater than Reference Halt Threshold
- Bit 19: **CH19 Reference Halt Flag**
  - 0: CH19 Normalised Delta less than Reference Halt Threshold
  - 1: CH19 Normalised Delta greater than Reference Halt Threshold

A.4 Activation Flags (0x100A)

Bit	31	30	29	28	27	26	25	24
Description	Reserved							
Default	0							

Bit	23	22	21	20	19	18	17	16
Description	Reserved				CH19 Activation Flag	CH18 Activation Flag	CH17 Activation Flag	CH16 Activation Flag
Default	0				0	0	0	0

Bit	15	14	13	12	11	10	9	8
Description	CH15 Activation Flag	CH14 Activation Flag	CH13 Activation Flag	CH12 Activation Flag	CH11 Activation Flag	CH10 Activation Flag	CH9 Activation Flag	CH8 Activation Flag
Default	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Description	CH7 Activation Flag	CH6 Activation Flag	CH5 Activation Flag	CH4 Activation Flag	CH3 Activation Flag	CH2 Activation Flag	CH1 Activation Flag	CH0 Activation Flag
Default	0	0	0	0	0	0	0	0

- Bit 0: **CH0 Activation Flag**
  - 0: CH0 Inactive
  - 1: CH0 Active
- Bit 1: **CH1 Activation Flag**
  - 0: CH1 Inactive
  - 1: CH1 Active
- Bit 2: **CH2 Activation Flag**
  - 0: CH2 Inactive
  - 1: CH2 Active
- Bit 3: **CH3 Activation Flag**
  - 0: CH3 Inactive
  - 1: CH3 Active
- Bit 4: **CH4 Activation Flag**
  - 0: CH4 Inactive
  - 1: CH4 Active
- Bit 5: **CH5 Activation Flag**
  - 0: CH5 Inactive
  - 1: CH5 Active
- Bit 6: **CH6 Activation Flag**
  - 0: CH6 Inactive
  - 1: CH6 Active
- Bit 7: **CH7 Activation Flag**
  - 0: CH7 Inactive
  - 1: CH7 Active
- Bit 8: **CH8 Activation Flag**
  - 0: CH8 Inactive
  - 1: CH8 Active
- Bit 9: **CH9 Activation Flag**
  - 0: CH9 Inactive
  - 1: CH9 Active
- Bit 10: **C1H0 Activation Flag**
  - 0: CH10 Inactive
  - 1: CH10 Active
- Bit 11: **CH11 Activation Flag**
  - 0: CH11 Inactive

- 1: CH11 Active
- Bit 12: **CH12 Activation Flag**
  - 0: CH12 Inactive
  - 1: CH12 Active
- Bit 13: **CH13 Activation Flag**
  - 0: CH13 Inactive
  - 1: CH13 Active
- Bit 14: **CH14 Activation Flag**
  - 0: CH14 Inactive
  - 1: CH14 Active
- Bit 15: **CH15 Activation Flag**
  - 0: CH15 Inactive
  - 1: CH15 Active
- Bit 16: **CH16 Activation Flag**
  - 0: CH16 Inactive
  - 1: CH16 Active
- Bit 17: **CH17 Activation Flag**
  - 0: CH17 Inactive
  - 1: CH17 Active
- Bit 18: **CH18 Activation Flag**
  - 0: CH18 Inactive
  - 1: CH18 Active
- Bit 19: **CH19 Activation Flag**
  - 0: CH19 Inactive
  - 1: CH19 Active

A.5 System Control (0x2000)

Bit	15	14	13	12	11	10	9	8
Description	Reserved						Sample Max Delta	Standby Mode
Default	0						0	0

Bit	7	6	5	4	3	2	1	0
Description	Software Reset	Acknow-ledge Reset	Execute Calibra-tion	Execute ATI	Reseed	Power Mode Selection		Re-configure Device
Default	0	0	0	0	0	0		0

- Bit 0: **Reconfigure Device**
  - Apply the device and channel configurations to the active configuration of the device, applying all settings defined in previous I^2C transactions.
  - Automatically cleared after instruction has been received
- Bits 1-2: **Power Mode Select**
  - 0: Normal Power
  - 1: Low Power
  - 2: Ultra-Low Power
  - 3: Automatic Power Modes
- Bit 3: **Reseed**
  - Set the LTA of each channel equal to the linearised counts value of that channel
  - Automatically cleared after instruction has been received
- Bit 4: **Execute ATI**
  - Execute the ATI sequence for each channel to obtain raw count values closest to the selected ATI target value
  - Automatically cleared after instruction has been received
- Bit 5: **Execute Automatic Calibration**
  - Execute the automatic calibration sequence for each channel to estimate the total key travel of all active channels
  - Automatically cleared after instruction has been received
- Bit 6: **Acknowledge Reset**

- Acknowledge the device reset and clear the reset flag in the system status register
- Automatically cleared after instruction has been received

› Bit 7: **Software Reset**
- Reset the device

› Bit 8: **Standby Mode**
- 0: Device is in normal operating mode
- 1: Device is in standby mode

› Bit 9: **Sample Max Delta**
- 0: Do not compare the delta value to the sampled max delta register
- 1: Compare the delta value to the sampled max delta register

A.6 System Configuration (0x2002)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	Enable Event Mode	Enable External Clock	Enable Trigger-Max™	Enable Reset Pin	Enable Event Pin	Enable Process-ing	Enable Individual Thresh-olds
Default	0	1	0	1	1	1	1	0

Bit	7	6	5	4	3	2	1	0
Description	Calibration on ATI	Calibration Enabled	ATI on Configure	ATI on Error	ATI Enabled	Scan on Comms	Wake on Activation	Wake on I^2C
Default	0	0	1	0	1	0	1	1

› Bit 0: **Wake on I^2C**
- 0: In automatic power mode, remain in LP/ULP on I2C transaction
- 1: In automatic power mode, return to NP on I2C transaction

› Bit 1: **Wake on activation**
- 0: In automatic power mode, remain in LP/ULP on channel activation
- 1: In automatic power mode, return to NP on channel activation

› Bit 2: **Scan on Comms**
- 0: Execute analog sampling without regard for I^2C transactions
- 1: Complete a single analog sample after receiving a complete I^2C transaction

› Bit 3: **ATI Enabled**
- 0: ATI sequence will never affect the multiplier and divider selection for any channel
- 1: ATI is enabled and will modify the multiplier and divider selection for active channels when the sequence is called

› Bit 4: **ATI on Error**
- 0: Device will not automatically start a new ATI sequence for channels that are outside their ATI band and display an ATI error flag
- 1: The device will automatically start a new ATI sequence for channels that are outside their ATI band and display an ATI error flag

› Bit 5: **ATI on Configure**
- 0: Do not modify channel multiplier and divider selection after reconfigure bit has been set in the system control register
- 1: Enter ATI sequence as the device is reconfigured to modify the channel multiplier and divider selections to achieve a raw counts value similar to the selected ATI target

› Bit 6: **Calibration Enabled**
- 0: Calibration sequences will never occur and the normalization value of all channels will remain unaffected
- 1: Calibration sequences are enabled and will affect the normalization value of all active channels

› Bit 7: **Calibration on ATI**
- 0: Calibration sequences will not automatically occur after ATI sequences have been completed and will require external instructions to occur
- 1: Calibration sequences will automatically occur after ATI sequences have been completed

› Bit 8: **Enable Individual Thresholds**
- 0: Select global channel activation threshold
- 1: Select activation threshold from individual activation threshold array

› Bit 9: **Enable Processing**

- 0: The device will not calculate values such as LTA or normalized delta and will only sample raw counts. This greatly increases the sample rate.
- 1: The device will process raw counts

> Bit 10: **Enable Event Pin**
- The device will pull the event pin low on channel activation events if the enable event pin is set

> Bit 11: **Enable Reset Pin**
- The device will pull the reset pin low when the reset flag is set in the system status register if the enable reset pin bit is set

> Bit 12: **Enable TriggerMax™**
- 0: TriggerMax™ UI will not affect activation flags
- 1: TriggerMax™ UI will track normalised delta values and set or clear activation flags

> Bit 13: **Enable External POSC Clock Source**
- 0: On-chip POSC oscillator is used as POSC clock source
- 1: Clock source provided on GPIO2 is used as POSC clock source

> Bit 14: **Enable Event Mode**
- 0: When GPIO sequences are enabled, the device will enter standby mode (See Section 7.3)
- 1: When GPIO sequences are enabled, the device will enter event mode.(See Section 7.3)

A.7 Multiplier and Divider Selection (0x3000 - 0x3026)

Bit	15	14	13	12	11	10	9	8
Description	Fine Multiplier		Fine Divider					Coarse Multiplier
Default	1		7					7

Bit	7	6	5	4	3	2	1	0
Description	Coarse Multiplier			Coarse Divider				
Default	7			7				

> Bit 0-4: **Coarse Divider**
- 5-bit value

> Bit 5-8: **Coarse Multiplier**
- 4-bit value

> Bit 9-13: **Fine Divider**
- 5-bit value

> Bit 14-15: **Fine Multiplier**
- 2-bit value

A.8 Calibration Parameters (0x3028 - 0x304E)

Bit	15	14	13	12	11	10	9	8
Description	Calibration Correction							
Default	0							

Bit	15	14	13	12	11	10	9	8
Description	Calibration Step							
Default	0							

> Bit 0-7: **Calibration Step**
- 8-bit value

> Bit 8-15: **Calibration Correction**
- 8-bit value

A.9 Channel Disable (0x3106)

Bit	31	30	29	28	27	26	25	24
Description	Reserved							
Default	0							

Bit	23	22	21	20	19	18	17	16
Description	Reserved				CH19 Disable	CH18 Disable	CH17 Disable	CH16 Disable
Default	0				0	0	0	0

Bit	15	14	13	12	11	10	9	8
Description	CH15 Disable	CH14 Disable	CH13 Disable	CH12 Disable	CH11 Disable	CH10 Disable	CH9 Disable	CH8 Disable
Default	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Description	CH7 Disable	CH6 Disable	CH5 Disable	CH4 Disable	CH3 Disable	CH2 Disable	CH1 Disable	CH0 Disable
Default	0	0	0	0	0	0	0	0

- Bit 0: **CH0 Disable**
  - 0: CH0 will complete analogue samples and update channel data registers
  - 1: CH0 will not complete analogue samples and data registers will remain zero
- Bit 1: **CH1 Disable**
  - 0: CH1 will complete analogue samples and update channel data registers
  - 1: CH1 will not complete analogue samples and data registers will remain zero
- Bit 2: **CH2 Disable**
  - 0: CH2 will complete analogue samples and update channel data registers
  - 1: CH2 will not complete analogue samples and data registers will remain zero
- Bit 3: **CH3 Disable**
  - 0: CH3 will complete analogue samples and update channel data registers
  - 1: CH3 will not complete analogue samples and data registers will remain zero
- Bit 4: **CH4 Disable**
  - 0: CH4 will complete analogue samples and update channel data registers
  - 1: CH4 will not complete analogue samples and data registers will remain zero
- Bit 5: **CH5 Disable**
  - 0: CH5 will complete analogue samples and update channel data registers
  - 1: CH5 will not complete analogue samples and data registers will remain zero
- Bit 6: **CH6 Disable**
  - 0: CH6 will complete analogue samples and update channel data registers
  - 1: CH6 will not complete analogue samples and data registers will remain zero
- Bit 7: **CH7 Disable**
  - 0: CH7 will complete analogue samples and update channel data registers
  - 1: CH7 will not complete analogue samples and data registers will remain zero
- Bit 8: **CH8 Disable**
  - 0: CH8 will complete analogue samples and update channel data registers
  - 1: CH8 will not complete analogue samples and data registers will remain zero
- Bit 9: **CH9 Disable**
  - 0: CH9 will complete analogue samples and update channel data registers
  - 1: CH9 will not complete analogue samples and data registers will remain zero
- Bit 10: **C1H0 Disable**
  - 0: CH10 will complete analogue samples and update channel data registers
  - 1: CH10 will not complete analogue samples and data registers will remain zero
- Bit 11: **CH11 Disable**
  - 0: CH11 will complete analogue samples and update channel data registers
  - 1: CH11 will not complete analogue samples and data registers will remain zero
- Bit 12: **CH12 Disable**
  - 0: CH12 will complete analogue samples and update channel data registers

- 1: CH12 will not complete analogue samples and data registers will remain zero

- Bit 13: **CH13 Disable**
  - 0: CH13 will complete analogue samples and update channel data registers
  - 1: CH13 will not complete analogue samples and data registers will remain zero
- Bit 14: **CH14 Disable**
  - 0: CH14 will complete analogue samples and update channel data registers
  - 1: CH14 will not complete analogue samples and data registers will remain zero
- Bit 15: **CH15 Disable**
  - 0: CH15 will complete analogue samples and update channel data registers
  - 1: CH15 will not complete analogue samples and data registers will remain zero
- Bit 16: **CH16 Disable**
  - 0: CH16 will complete analogue samples and update channel data registers
  - 1: CH16 will not complete analogue samples and data registers will remain zero
- Bit 17: **CH17 Disable**
  - 0: CH17 will complete analogue samples and update channel data registers
  - 1: CH17 will not complete analogue samples and data registers will remain zero
- Bit 18: **CH18 Disable**
  - 0: CH18 will complete analogue samples and update channel data registers
  - 1: CH18 will not complete analogue samples and data registers will remain zero
- Bit 19: **CH19 Disable**
  - 0: CH19 will complete analogue samples and update channel data registers
  - 1: CH19 will not complete analogue samples and data registers will remain zero

A.10 Timing Generator Settings (0x3146)

Bit	15	14	13	12	11	10	9	8
Description	Timing Generator Period 2							
Default	0							

Bit	7	6	5	4	3	2	1	0
Description	Timing Generator Period 1							
Default	0							

- Bit 0-7: **Timing Generator Period 1**
  - Charge Phase Period
  - Tx pins charged to V_{REG}
- Bit 8-15: **Timing Generator Period 2**
  - Transfer Phase Period
  - Tx pins charged to V_{ss}
- Tx Signal Frequency = $\frac{F_{POSC}}{\text{Period}_1+\text{Period}_2+2}$
- Tx Signal Duty Cycle = $\frac{\text{Period}_1+1}{\text{Period}_1+\text{Period}_2+2}$
- The Tx signal is only affected when the *Enable Tx Prescaler* bit is set in the *Hardware Settings* register

A.11 Hardware Settings (0x3148)

Bit	15	14	13	12	11	10	9	8
Description	Reserved						Initialisation Length	
Default	0						1	

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Enable Tx Prescaler	Discharge 0.5V	Mutual Induc-tance	Static Multiplier	Max Count Select		
Default	0	0	0	0	1	4		

- Bit 0-2: **Max Count Select**
  - Select the maximum value raw count that can be sampled
  - Limits the maximum time that can be used to complete a conversion
  - 0: 383
  - 1: 511
  - 2: 787
  - 3: 1023
  - 4: 2047
  - 5: 4095
  - 6: 8191
- Bit 3: **Coarse Input Multiplier Static**
  - 0: Disabled
  - 1: Enabled
- Bit 4: **Mutual Inductance Mode**
  - 0: Disabled
  - 1: Enabled
- Bit 5: **Discharge 0v5**
  - 0: Discharge Cs to 0V
  - 1: Discharge Cs to 0.5V
- Bit 6: **Enable Tx Prescaler**
  - 0: Tx frequency equal to F_{POSC} (16MHz)
  - 1: Tx frequency equal to conversion frequency defined by timing generator periods
- Bit 8-9: **Initialisation Length**
  - 0: 16
  - 1: 32
  - 2: 64
  - 3: 256

B Code Examples

B.1 GPIO Sequence: Key Scan

```
void scan_keys()
{
    for (uint8_t i = 0; i < NR_COLUMNS; i++)
    {
        // Set C0 LOW
        GPIO_write(columns[i].c0, 0);
        delay_us(20);

        // Read reset and ATI error states
        for (uint8_t j = 0; j < NR_ROWS; j++)
        {
            iqs9320_data[i][j].reset = GPIO_read(rows[j].r1);
            iqs9320_data[i][j].ati_error = GPIO_read(rows[j].r2);
        }

        // Scan 20 channels with key scanning
        for (uint8_t j = 0; j < 5; i++)
        {
            if (j%2)
            {
                // Set C0 LOW
                GPIO_write(columns[i].c0, 0);
            }
            else
            {
                // Set C0 HIGH
                GPIO_write(columns[i].c0, 1);
            }

            delay_us(20);

            // Read channel states
            for (uint8_t k = 0; k < NR_ROWS; k++)
            {
                iqs9320_data[i][k].channels[j*4 + 0] = GPIO_read(rows[k].r0);
                iqs9320_data[i][k].channels[j*4 + 1] = GPIO_read(rows[k].r1);
                iqs9320_data[i][k].channels[j*4 + 2] = GPIO_read(rows[k].r2);
                iqs9320_data[i][k].channels[j*4 + 3] = GPIO_read(rows[k].r3);
            }
        }

        // Set C0 LOW - Exit key scan state
        GPIO_write(columns[i].c0, 0);
        delay_us(20);

        // Set C0 HIGH - Return to default pin state
        GPIO_write(columns[i].c0, 1);
        delay_us(20);
    }
}
```

B.2 GPIO Sequence: I²C Configuration

```
void config_mode_enter(uint8_t column_select, uint8_t row_select)
{
    // Set R0 LOW for the selected row
    GPIO_write(rows[row_select].r0, 0);

    // Set R3 LOW for all other rows
    for (uint8_t i = 0; i < NR_ROWS; i++)
    {
        if (i != row_select) GPIO_write(rows[i].r3, 0);
    }

    // Set C0 LOW
    GPIO_write(columns[column_select].c0, 0);
    delay_us(20);

    // Set C0 HIGH
    GPIO_write(columns[column_select].c0, 1);
    delay_us(20);

    // Set R0 HIGH for the selected row
    GPIO_write(rows[row_select].r0, 1);

    // Set R3 HIGH for all other rows
    for (uint8_t i = 0; i < NR_ROWS; i++)
    {
        if (i != row_select) GPIO_write(rows[i].r3, 1);
    }

    // Await R1 falling edge - 1ms timeout
    for (uint8_t i = 0; i < 50; i++)
    {
        if (GPIO_read(rows[row_select].r1) == 0) break;
        delay_us(20);
    }
}

void config_mode_exit(uint8_t row_select)
{
    // Set R0 LOW
    GPIO_write(rows[row_select].r0, 0);

    // Await R1 rising edge - 1ms timeout
    for (uint8_t i = 0; i < 50; i++)
    {
        if (GPIO_read(rows[row_select].r1) == 1) break;
        delay_us(20);
    }

    // Set R0 HIGH
    GPIO_write(rows[row_select].r0, 1);
}
```

B.3 GPIO Sequence: Event/Standby Mode

```
void event_standby_mode_enter()
{
    // R0 LOW for all rows
    for (uint8_t i = 0; i < NR_ROWS; i++){
        GPIO_write(rows[i].r0, 0);
    }
    delay_us(20);

    // C0 LOW for all columns
    for (uint8_t i = 0; i < NR_COLUMNS; i++){
        GPIO_write(columns[i].c0, 0);
    }
    delay_us(20);

    // R0 HIGH for all rows
    for (uint8_t i = 0; i < NR_ROWS; i++){
        GPIO_write(rows[i].r0, 1);
    }
    delay_us(20);

    // C0 HIGH for all columns
    for (uint8_t i = 0; i < NR_COLUMNS; i++){
        GPIO_write(columns[i].c0, 1);
    }
    delay_us(20);
}

void event_standby_mode_exit()
{
    // R0 LOW for all rows
    for (uint8_t i = 0; i < NR_ROWS; i++){
        GPIO_write(rows[i].r0, 0);
    }
    delay_us(20);

    // C0 LOW for all columns
    for (uint8_t i = 0; i < NR_COLUMNS; i++){
        GPIO_write(columns[i].c0, 0);
    }
    delay_us(20);

    // Write I2C data
    uint8_t i2c_write_data[] = {0x00};
    i2c_write(0x30, i2c_write_data, 1);
    delay_us(500);

    // R0 HIGH for all rows
    for (uint8_t i = 0; i < NR_ROWS; i++){
        GPIO_write(rows[i].r0, 1);
    }

    // C0 HIGH for all columns
    for (uint8_t i = 0; i < NR_COLUMNS; i++){
        GPIO_write(columns[i].c0, 1);
    }
}
```

C Calibration Procedures

C.1 Automatic Calibration

C.2 Manual Calibration

One-time calibration procedure:

- Run ATI on IQS9320
- Read and store ATI parameters of each channel
- Press down each key fully
- Read and store the *Sampled Max Delta* value of each channel

Start-up configuration procedure:

- Disable ATI
- Write the stored ATI parameters for each channel
- Set the *Effective Max Delta* parameter for each channel

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